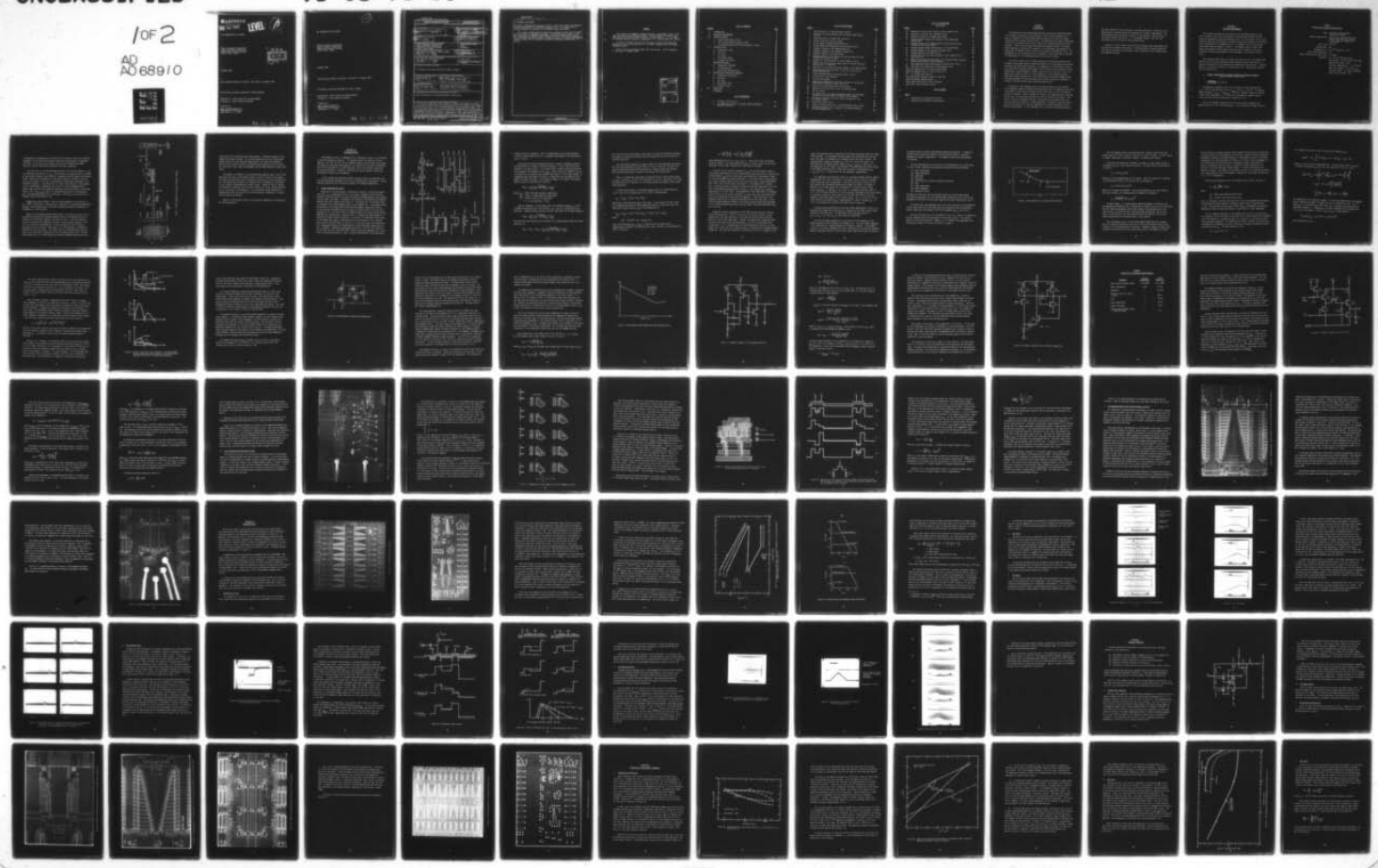
AD-A068 910 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 9/5
CCD PROCESSOR FOR INSB ARRAY.(U)
DEC 78 R J KANSY N00173-76-C-0237
UNCLASSIFIED TI-08-78-50 NL

1 OF 2
AD A068910



LEVEL B

CCD PROCESSOR FOR InSb ARRAY

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75265

December 1978

Final Technical Report for Period 1 June 1976 - 31 October 1978

Distribution Unlimited, Approved for Public Release

Sponsored by: Naval Electronic Systems Command
Directed by: Naval Research Laboratory

Prepared for

Naval Research Laboratory
4555 Overlook Avenue, S.W.
Washington, D. C. 20375

13

CCD PROCESSOR FOR InSb ARRAY

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75265

December 1978

Final Technical Report for Period 1 June 1976 - 31 October 1978

Distribution Unlimited, Approved for Public Release

Sponsored by: Naval Electronic Systems Command
Directed by: Naval Research Laboratory

Prepared for

Naval Research Laboratory
4555 Overlook Avenue, S.W.
Washington, D. C. 20375

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE *(and Subtitle)*

(6) CCD PROCESSOR FOR InSb ARRAY.

5. TYPE OF REPORT & PERIOD COVERED

(9) Final Technical Report.
1 June 1976 - 31 October 1978.

6. PERFORMING ORG. REPORT NUMBER

08-78-50

7. AUTHOR(s)

(10) Robert J. Kansy

8. CONTRACT OR GRANT NUMBER(s)

(15) N00173-76-C-0237

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75265

403 833

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

62762N
XF54583004

11. CONTROLLING OFFICE NAME AND ADDRESS

Naval Electronic Systems Command N00039
Code 304, L. W. Sumney
Washington, D. C. 20360

(11)

12. REPORT DATE

December 1978

13. NUMBER OF PAGES

117

14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*

Naval Research Laboratory N00173
Code 5262, Dr. W. D. Baker
Washington, D. C. 20375

15. SECURITY CLASS. *(of this report)*

Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Distribution unlimited, approved for public release.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

(12) 129 p. (14) TI-08-78-50

18. SUPPLEMENTARY NOTES

(16) F54583 (17) XF54583004

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Focal Plane Arrays, IR Signal Processing, InSb Arrays

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

→ A silicon integrated circuit employing n-channel MOS (NMOS) and charge-coupled device (CCD) circuits has been designed and fabricated for the purpose of interfacing with an InSb infrared detector array on the focal plane. The resulting focal plane array is a fully parallel implementation of the concept introduced by Milton and Hess [A. F. Milton and M. Hess, "Series-Parallel Scan IR CID Focal Plane Array Concept," Proceedings of 1975 International Conference on the Application of Charge Coupled Devices, San Diego, CA, October 1975, pp. 71-83] and includes preamplification, correlated double sampling, and

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

UNCLASSIFIED 403 833
SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

20. ABSTRACT (Continued)

16-element time-delay-and-integration (TDI) for each of 24 channels corresponding with the assumed 16 x 24 element detector array. The signals from individual channels are combined in a 24-channel output multiplexer.

This report includes details related to the design of each circuit element and the results of subsequent evaluation. Key problem areas related to cryogenic application of standard analog NMOS circuits are reported and analyzed. It is concluded that NMOS circuitry is ideally suited for cryogenic applications, although further work is required to completely characterize alternative circuits.

PREFACE

This report was prepared by Texas Instruments Incorporated, Dallas, Texas, under Navy Contract No. N00173-76-C-0237. The work under this contract was administered and funded by Naval Electronic Systems Command. Dr. W. D. Baker of the Naval Research Laboratory, Washington, D. C., was the Scientific Officer.

At Texas Instruments the work was performed in the Advanced Technology Laboratory under the direction of Dr. C. R. Hewes, Manager of the CCD Signal Processing branch.

This is the Final Technical Report for the contract. It was submitted by the author in December 1978.

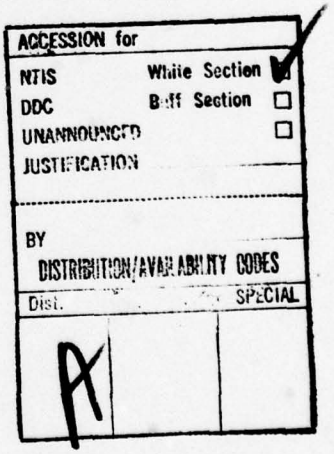


TABLE OF CONTENTS

LIST OF APPENDIXES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

(Continued)

LIST OF TABLES

SECTION I
INTRODUCTION

The objective of the program executed under Contract No. N00173-76-C-0237 is the design, fabrication, and testing of a silicon signal processor chip that is intended for on-focal plane operation with an intrinsic InSb charge injection device infrared detector array. The combined use of these technologies results in a realization of the focal plane array concept developed by Milton and Hess.[1] The silicon processor chip provides preamplification, correlated double sampling, time delay and integration, dc restoration, and output multiplexing for 24 channels from a single 16 x 24 element InSb detector array. The development of this integrated circuit represents an important step in the overall development of true second-generation tactical FLIR systems.

The initial stages of this program focussed on a detailed examination of processor requirements based on projected detector array performance and assumed prototype FLIR system specifications. The components of the processor circuit were individually analyzed and designed. This "building block" approach allowed optimization of each component, thereby lowering overall technical risk at the expense of a moderate level of circuit redundancy. The processor chip was fabricated using a double-level, self-aligned polysilicon gate CCD/NMOS process that was developed at Texas Instruments and has been successfully employed in a number of device analog signal processing applications.

Evaluation of the component test structures included with the processor chip indicated a number of problem areas associated with low temperature operation of the NMOS circuits and poor charge transfer efficiency in two of the charge transfer structures. Based on these test results, the components were redesigned and the test structures were modified to allow more detailed evaluation. Test results from the redesigned chip have illuminated two key problem areas that were not previously observed. Freeze-out effects in depletion load transistors have been observed at 77 K and are responsible for severe degradation of preamplifier performance. To our knowledge, this is the first time these effects

have been observed in MOS transistors, and they constitute a limitation to the application of standard analog MOS techniques at cryogenic temperatures. The second problem area involves an oversight in the analysis of noise sources in the charge transfer structures. It is concluded, however, that low risk alternatives exist for each of these problem areas.

Section II of this report describes the prototype system requirements and the resulting processor architecture. Following sections include design and test details for each of the processor chips, discussion of key problem areas, and proposed solutions.

SECTION II
PROCESSOR REQUIREMENTS

This section describes the derivation of the performance goals for the signal processor chip from the prototype FLIR system specifications and the electrical parameters of the InSb detector array. For the purpose of the signal processor technology development, a prototype system was assumed to be a horizontally scanned 525-line TV-compatible FLIR. A complete list of the prototype system specifications appears in Table 1. This paper system includes time-delay-and-integration (TDI) signal processing with 16 elements in the scan direction to provide approximately 12 dB improvement in the signal-to-noise ratio.

The prototype focal plane array (FPA) consists of ten 16 x 24 element InSb detector arrays with an associated signal processor chip for each array. To preserve horizontal MTF, the detectors are sampled $2\frac{1}{4}$ times per dwell. Detector spacing is adjusted to provide 3:1 interleave for TDI. The detector sampling rate is obtained from

$$f_s = \frac{(\text{number samples/dwell})\ (\text{number horizontal resolution elements})}{(\text{scan efficiency})\ (\text{field time})}$$

$$= \frac{(2\frac{1}{4})\,(480)}{(0.7)\,(1/60)} = 92.57 \text{ kHz} \quad .$$

The detector integration time is the reciprocal of the sampling rate, $\tau_{int} = 10.8\ \mu s$, and the dwell time is $\tau_{dwell} = 2\frac{1}{4}\ \tau_{int} = 24.3\ \mu s$. The maximum signal frequency is $f_{max} = 0.8/\tau_{dwell} = 32.9$ kHz. Detector operation requires a focal plane temperature of 77 K, and use with standard cryogenic coolers limits the total on-focal plane power dissipation to 1 W.

The use of CCD/NMOS technology for the silicon signal processor chip appears optimal for the following reasons: (1) the operation of NMOS circuitry

Table 1

Prototype FLIR System Specifications

Scan:	Horizontal Unidirectional 70% Scan Efficiency
Display Compatibility:	525-Line TV, 2:1 Interlace, 4/3 Aspect Ratio (480 res. elements in scan, 360 res. elements in cross-scan)
Dwell Time:	24.3 μs
Samples/Dwell:	$2\frac{1}{4}$
Background Flux:	5×10^{14} Photons/s - cm^2
Focal Plane Temperature:	77 K
Power Dissipation on Focal Plane:	1 W (max)
Detectors:	10 - 16 x 24 InSb CID Arrays
	Active Area: 4 $mils^2$ (2.58×10^{-5} cm^2)
	Quantum Efficiency: 50%
	Insulator Capacitance: 3×10^{-8} F/cm^2
	Read Line Voltage: -6 to -8 V, nom
	Injection Pulse: +3 V, 85 ns duration
	Reset Pulse Duration: 50 ns

is enhanced at low temperatures,[2] whereas that of bipolar circuitry is typically degraded[3]; (2) the TDI and multiplexer functions are conveniently implemented with CCDs; (3) CID control and signal sensing are facilitated using NMOS amplifier circuits that exhibit extremely high input impedances.

The CID array is a self-multiplexed structure, thus all 16 detectors in the TDI column must be read out in τ_{int}. This results in a sampling rate of 1.48 MHz at each signal processor input terminal. Background-limited detector performance (BLIP) requires that fluctuations of the output signal be limited to the shot noise on the number of carriers in the detector charge packet generated by the background radiation. To achieve BLIP, all other noise sources in the processor circuit, when added in quadrature, must result in a noise component that is smaller than the shot noise component determined from the variance on the charge packet, $\langle\sigma^2\rangle = \eta\phi_B \tau_{int} A_d$ where η is the quantum efficiency of the detector, ϕ_B is the background photon flux in photons/s - cm^2 and A_d is the active (i.e., imaging) area of each detector cell.

Based on the data of Table 1, the shot noise component in rms carriers is $N_n = \langle\sigma^2\rangle^{\frac{1}{2}} = 264$ carriers. Note that N_n is based only on system requirements and detector specifications and will be used to evaluate processor performance requirements in a later section.

Based on the prototype system specifications, the signal processor chip is configured to provide the necessary preamplification, TDI processing and multiplexing for 24 detector channels from each CID array. The block diagram in Figure 1 illustrates the components included in each processor channel. This is a fully parallel implementation of the series-parallel scan FPA concept developed by Milton and Hess,[1] which results in a 24X decrease in preamplifier bandwidth and CDS clock rates. The RESET switch and INJECTION PULSE coupling capacitor are required for operation of the CID detector sense line. The low noise preamplifier is an NMOS design with negative feedback employed for small

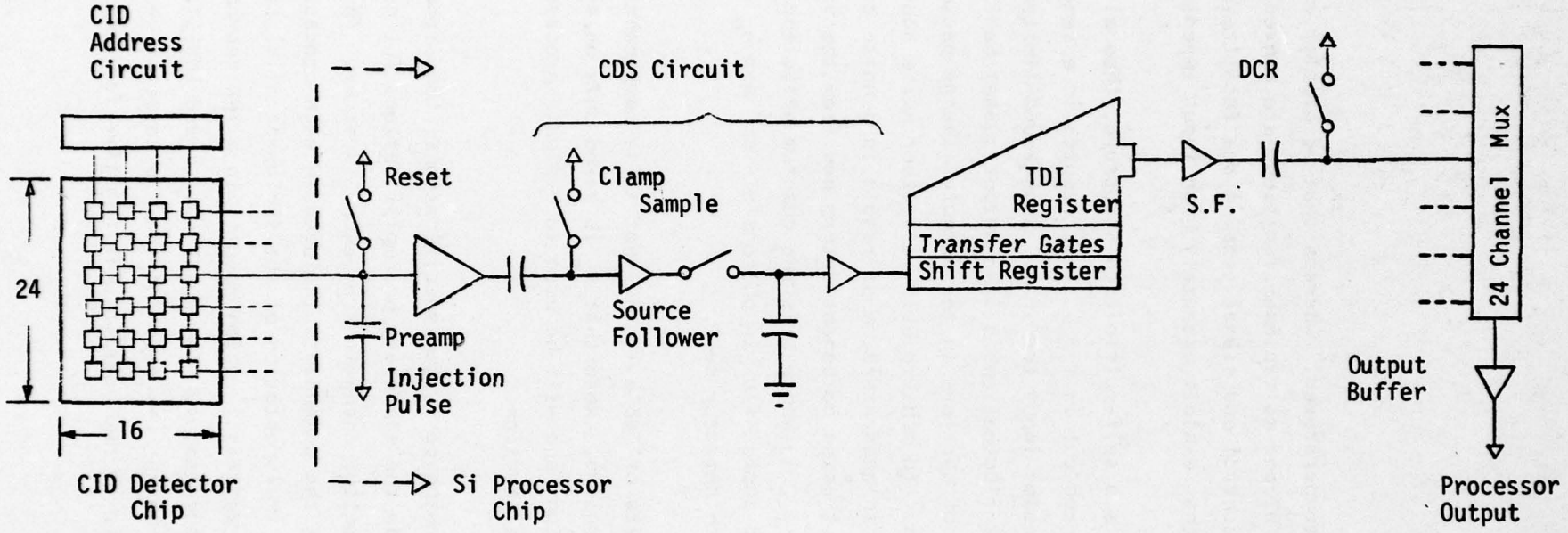


Figure 1 Block Diagram of a Single Processor Channel

signal gain and dc operating point stabilization. Significant aspects of the preamplifier design include: (1) low noise operation with the limited power budget required for on-focal-plane applications, (2) sufficient bandwidth and slew rate to allow settling of transients due to detector control pulses, (3) sufficient linear range to accommodate typical NMOS threshold voltage variations.

The preamp is followed by a correlated double sampling (CDS) circuit[2] that suppresses kTC noise on the detector sense line and 1/f noise in the preamp. The signal from the CDS circuit is applied to the input of a CCD TDI consisting of a 16-stage charge transfer shift register that is connected to a 48-stage CCD TDI register through parallel transfer gates. Charge in the TDI register is advanced one stage each time the shift register is filled, thereby matching the 3:1 interleave in the detectors. The ac couple/dc restore operation is accomplished at the TDI output and the 24 channels are recombined in a charge transfer output multiplexer.

Details of the design of each of the processor components are presented in the following section.

SECTION III
PROCESSOR DESIGN

The processor circuit is composed of six individual circuits, as illustrated in the block diagram in Figure 1: (1) detector sense line control, (2) preamplifier, (3) CDS, (4) TDI, (5) ac couple/dc restore, and (6) output multiplexer. The operation and design requirements of (1) through (3) are highly interrelated and will be considered as a single functional unit to facilitate a discussion of the design details. Similarly, discussion of the ac couple/dc restore and multiplexer circuits will be combined.

In this section the operational details of each circuit are described, and the resulting design parameters and circuit configurations are presented. Unless otherwise specified, all calculations assume a 77 K ambient temperature.

A. Signal Conditioning Circuit

Operation of the CID detector is depicted in Figure 2. During the integration time, τ_{int}, IR-generated carriers are stored in potential wells that are created in the InSb substrate by means of external voltages applied to the address line and sense line gates. The address line voltage is controlled by an external read-out scan shift register (see Figure 1). The sense line, on the other hand, is connected to the high impedance input of the preamplifier. To maintain control of the sense line voltage (which would otherwise depend, among other things, on the previous read operation and the amount of charge stored in all the cells connected to it), the reset switch is closed briefly prior to each charge sensing operation and reestablishes a reference level. Although the reset operation is required for proper detector operation, it results in an additional noise source at the preamplifier which is characterized by an uncertainty in the reference level given by $(kT/C_T)^{\frac{1}{2}}$ where, as before, C_T is the total sense line capacitance. This voltage uncertainty can be expressed as a noise equivalent charge given by $neq = (kTC_T)^{\frac{1}{2}}/q$. Assuming an approximate value for C_T (10 pF), this results in an neq of 650 carriers, $2\frac{1}{2}$ times larger than the shot noise component, N_n, calculated in the previous section. Thus, in order to achieve BLIP, the reset noise

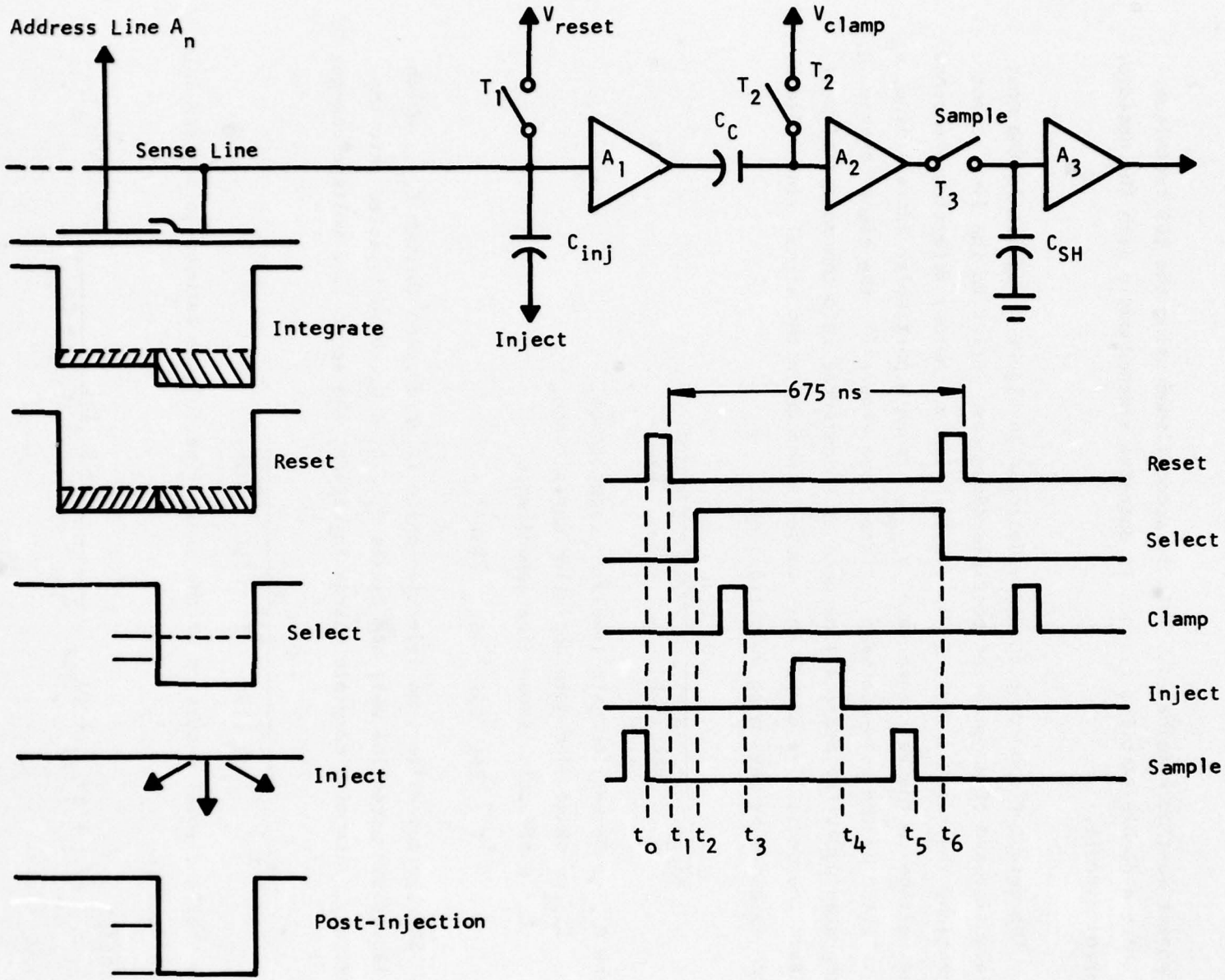


Figure 2 Operation of the CID Detector and the Signal Conditioning Circuit

component must be eliminated. This is accomplished using the CDS technique, in which a double sampling circuit is operated synchronously with the detector control circuit.

The detector operating sequence depicted in Figure 2 represents the most straightforward of a number of possible sequences. Prior to the line select operation, the reset switch, T, is closed briefly, thereby resetting the sense line voltage to the reference level V_{reset}. When a particular address line, A_n, is selected by the read-out scan register (see Figure 1), the signal charge, Q, integrated under the address line gate is transferred into the potential well beneath the sense line gate. This causes a change in the signal line voltage, which is given by (assuming hole transfer):

$$\Delta V_{SL1} = \frac{Q_1 \, C_{ISL}}{C_{DSL} \, C_{ISL} + C_T' \, (C_{ISL} + C_{DSL})} \quad ,$$

where C_{ISL} = sense line gate insulator capacitance,
C_{DSL} = sense line gate depletion capacitance,
C_T' = effective sense line capacitance
$= C_T - C_{ISL} \, C_{DSL}/(C_{ISL} + C_{DSL})$.

Shortly thereafter, an injection pulse is ac-coupled through C_{inj}, which collapses the potential well and causes $Q_s = Q_1 + Q_2$ to be injected into the substrate. Assuming complete charge injection, the sense line voltage changes by

$$\Delta V_{SL2} = \frac{- Q_2 \, C_{ISL}}{C_{DSL} \, C_{ISL} + C_T' \, (C_{ISL} + C_{DSL})} \quad .$$

Note that the total excursion of the sense line voltage between select and inject operations is

$$\Delta V_{SL} = \Delta V_{SL1} - \Delta V_{SL2} = \frac{Q_{sig} \, C_{ISL}}{C_{DSL} \, C_{ISL} + C_T' \, (C_{ISL} + C_{DSL})}$$

thus, sensing the entire detector signal requires forming the difference between two samples, one acquired following the select operation and one following the injection operation.

Correlated double sampling is used to remove the noise component associated with the reset operation on the CID sense line and, in addition, performs the sample-differencing operation discussed above. Figure 2 shows the timing of the clamp and sample pulses relative to the select and inject pulses.

When T_1 is opened the input mode is characterized by a time constant given by $R_{off}\ C_T$, where R_{off} is the "off" resistance of T_1 and is typically $> 10^{10}$ ohms. The reset noise will, therefore, be correlated between any samples taken between reset operations.

If the clamp operation is performed between select and inject operation, it will result in a voltage stored on C_C, which is approximately

$$V_{C_C} = V_{clamp} - A_1(V_R + SV_R + \Delta V_{SL1}) \quad ,$$

where SV_R is the uncertainty due to the reset. If the output of buffer stage A_2 is sampled following the inject operation and prior to the next reset, the resulting voltage stored on C_{SH} will be proportional to

$$V_{C_{SH}} = V_{clamp} - A_1(V_R + SV_R + \Delta V_{SL1}) + A_1(V_R + SV_R' + \Delta V_{SL2})$$

where

$$SV_R' = SV_R \exp[-(t_s - t_3)/R_{off}\ C_T] \quad .$$

Thus, the difference $\Delta V_{SL2} - \Delta V_{SL1}$ is obtained and the reset noise is approximately cancelled. The observed noise level, referred to the preamplifier input, is given by

$$e_n = \left(\frac{kT}{C_T}\right)^{\frac{1}{2}} \left\{2\left(1 - \exp\left[-\frac{(t_5 - t_3)}{R_{off}\, C_T}\right]\right)\right\}^{\frac{1}{2}} ,$$

which approaches zero for $t_5 - t_3 \ll R_{off}\, C_T$. Note that if the time between clamp and sample is too long compared to $R_{off}\, C_T$, the correlation of the noise decreases, and the input referred noise can actually increase.

The value of the injection capacitor C_{inj} must be sufficiently large to allow modest requirements for the injection pulse amplitude, which is capacitively divided between C_{inj} and the input node capacitance due to the detector signal line and the preamplifier input capacitance. On the other hand, large values of C_{inj} cause increased loading of the input node resulting is signal attenuation and a lower input referred noise requirement in the preamplifier to achieve BLIP. Projected detector parameters indicate the maximum capacitance (all wells full) of the detector signal line will be C_{SL} = 6 pF, based on an insulator capacitance of 3×10^{-8} F/cm^2. The preamplifier input capacitance is predicted to be in the 2 to 3 pF range, resulting in a worst-case input node capacitance of 8 to 9 pF exclusive of the injection capacitor. Proper operation of the detectors requires a 3 V injection pulse amplitude on the input node. Use of a 3 pF injection capacitor results in an injection pulse amplitude requirement of 12 V on the injection pulse bus line and a total input node capacitance (C_T) of 11 to 12 pF.

Selection of design parameters for the RESET switch transistor involves similar considerations. The W/L ratio must be sufficiently large to allow completion of the reset operation in the required interval (50 ns) and with realistic control pulse amplitudes. However, the gate-source capacitance adds directly to the total input node capacitance, C_T, and a minimum gate width is desirable. If it is assumed that the reset operation occurs prior to line select, and further that the injection process is complete (all integrated charge recombines), then the reset operation is required to correct for changes in the

signal line potential due to injection of the charge integrated under the signal line electrode. If the address line and signal line electrodes have the same area, the signal line potential will change by half the signal voltage. The maximum signal voltage corresponds to a "full well" under the signal line electrode, and the maximum signal charge is $Q_{max} = V_{inj}\ C_{SL}'$, where C_{SL}' is the capacitance of one signal line electrode. The maximum drain-source voltage on the RESET transistor prior to the reset operation is approximately $V_{DS} = V_{inj}\ C_{SL}'/2\ C_T'$, or about 50 mV for the parameters assumed above.

An incomplete reset operation results in crosstalk between adjacent samples. Assuming that less than 1% crosstalk is desirable, the W/L ratio of the RESET switch transistor can be determined. Since the drain-source voltage will be much smaller than the applied gate-source voltage, the device is assumed to operate in the triode region and is modelled as a resistor having a value $1/G_{DS}$, where $G_{DS} = K\ (W/L)(V_{GS} - V_T)$, and K is a processing constant equal to 1.4×10^{-5} for short channel (W = 0.3 mil) devices fabricated at Texas Instruments. A 1% accuracy requires a reset interval of 4.6 times the effective RC time constant of the input node, which is simply C_T/G_{DS}. For C_T = 12 pF and a 50 ns reset interval the required G_{DS} is approximately 1.1 mmho. Assuming $V_{GS} - V_T$ = 5 V, the resulting W/L ratio for the reset switch is about 16.

The gate-source capacitance of this device adds approximately 0.5 pF to C_T. Note that this capacitance also results in coupling of the reset control pulse waveform to the sense line. The amplitude of this spurious signal is $V_{RP}\ C_{GS}/(C_{GS} + C_T)$, where V_{RP} is the reset pulse amplitude.

The low noise NMOS preamplifier is the most critical component on the signal processor chip and presents the highest risk. The use of NMOS technology in this application is deemed optimum for a number of reasons. Silicon NMOS circuitry is a natural candidate for direct interface with the InSb MIS detectors. Bipolar technology requires a static bias current supply that would be difficult

to provide without seriously compromising detector performance. In addition, whereas bipolar device performance (including junction FETs) is typically degraded at cryogenic temperatures, all aspects of MOS device performance are enhanced.

The key considerations in the design of the preamplifier are listed below in order of their importance to achieving the desired system performance:

(1) Noise performance
(2) Power dissipation
(3) Bandwidth
(4) Slew rate
(5) Insensitivity to ±100 mV threshold variations
(6) Gain
(7) Input capacitance
(8) Output impedance
(9) Required Si area.

Of these, only the first two are dictated directly by system requirements. The remaining parameters are interrelated among themselves as well as with the parameters of the other circuits that comprise the signal conditioning circuit.

To achieve BLIP, the quadrature sum of all noise sources in the preamplifier circuit, when referred to the input node, must be smaller than the equivalent noise voltage due to the detector shot noise component qN_n/C_T (rms volts).

The noise characteristics of the MOSFETs in the first stage of a preamplifier normally dominate the noise performance of the entire circuit. The spectral density of the noise equivalent voltage, e_n, in a MOSFET can be separated into two distinct regions of interest, as shown in Figure 3.

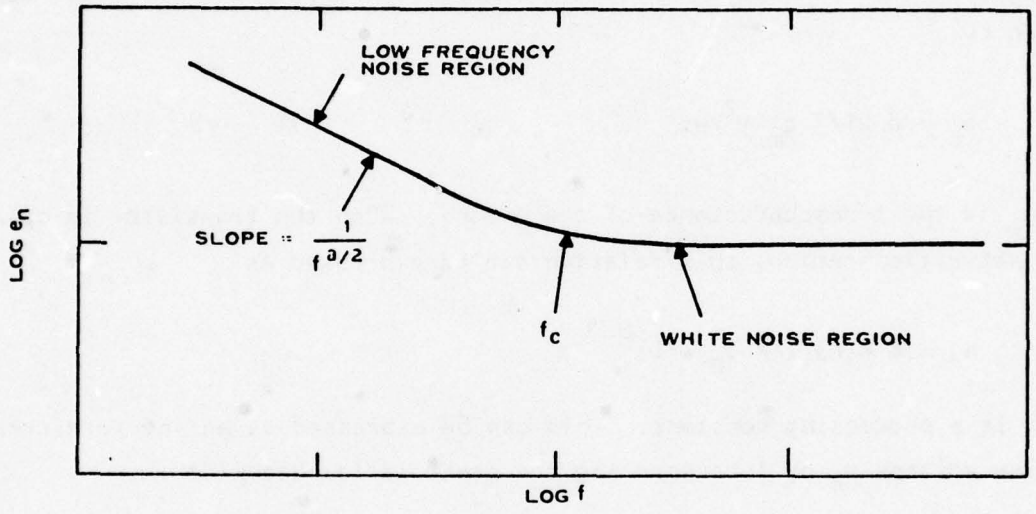


Figure 3 Noise Spectrum of a Typical MOS Transistor

The low frequency region is characterized by a spectral density function proportional to f^{-1} and is usually referred to as the 1/f region. The flat region at higher frequencies is the white, thermal, or Johnson-noise region.

The white noise generated in MOSFETs is caused by random thermal motion of the charge carriers in the conducting channel. The input referred noise density is given by

$$n_d = 8\ kT/3\ g_m\ V^2/Hz \quad ,$$

where g_m is the transconductance of the device. When the transistor is operated in the saturation region, this relation can be expressed as

$$n_d = 8\ kT/3\ (2K\ I_D\ W/L)^{\frac{1}{2}} \quad ,$$

where K is a processing constant. This can be expressed as an input referred rms noise voltage v_n by incorporating the preamplifier bandwidth:

$$v_n = \left(\frac{8\ kT\ BW}{3}\right)^{\frac{1}{2}} \left(2K\ I_D\ W/L\right)^{-\frac{1}{4}} \quad .$$

The gate length, L, is constrained by photolithographic limitations, and the preamplifier bandwidth, BW, is determined by the CDS circuit (to be discussed). The only remaining parameters that affect Johnson noise performance are the drain current, I_D, which directly influences power dissipation, and the gate width, W, which affects the input capacitance and the required silicon area. These considerations are discussed later in this section.

The low-frequency noise in the surface-channel MOSFET device is caused mainly by random fluctuations of carriers in the fast-interface surface states located at the oxide-semiconductor interface. Although a number of authors have discussed the characteristics of surface-state noise in the MOSFET, no closed

form solution has yet been achieved, mainly because of difficulties in obtaining a unique relation to the processing of the device. Possibly the most reasonable explanation is based on the modification of a noise model originally introduced by McWhorter[7] for the explanation of flicker or 1/f noise in bulk semiconductors. This modification has been extensively evaluated by other investigators[8,9] under the assumption that the noise is caused by a random trapping of free carriers in the fast-interface surface states. To provide the observed 1/f frequency response, the trapping is postulated to occur via a tunneling mechanism. This, then, results in the low frequency fluctuation in the channel current with a $(1 + \omega^2 \tau^2)^{-1}$ dependence.

The generalized expression for low-frequency noise in MOS transistors is

$$e_n = \frac{q}{C_{ox}} \frac{N_{ss}}{\alpha f WL} F(V_{GS}) \quad ,$$

where

C_{ox} = gate oxide capacitance/unit area,

N_{ss} = surface state density/unit area,

and α is a constant related to the statistics of the noise mechanism and depends on the particular model employed, although a typical value is approximately $\alpha = 80$. The additional multiplicative factor $F(V_{GS})$ accommodates the observed dependence on gate voltage that exhibits a square root to linear dependence.

The 1/f component generated in the preamplifier circuit is not expected to be problematic due to the effect of the CDS circuit, which substantially suppresses the noise generated at frequencies below $1/\Delta t$, where Δt is the interval between clamp and sample operation. To understand this effect, consider the noise to be an ensemble of independent sine wave of arbitrary frequency and phase and having average amplitude e_{av}. The input waveform is then

$$e_{in} = e_{av} \sin(\omega t + \phi) \quad .$$

The response of the CDS circuit to a particular component ω_o is

$$e_{out}(t) = e_{av} \sum_{n=-\infty}^{\infty} \left[\sin(n\omega_o T_s + \phi) - \sin(n\omega_o T_s - \omega_o \Delta t + \phi)\right] \quad ,$$

where T_s is the inverse of the sample rate. The mean square value of $e_{out}(\omega)$ is found by integrating $e_{out}^2(\omega)$ over all values of ϕ (0 to 2π). Thus,

$$\left[e_{out}(\omega)\right]_{rms} = e_{av}\left[\frac{1}{2\pi}\int_o^{2\pi}\frac{1}{2\pi}\left|\int_{-\infty}^{\infty} e_{out}(t)\, e^{-j\omega t}\, dt\right|^2 d\phi\right]^{\frac{1}{2}}$$

$$= e_{av}\left(1 - \cos\omega_o \Delta t\right)^{\frac{1}{2}}\left|\frac{\sin \omega T_s/2}{\omega T_s/2}\right|$$

$$\cdot \sum_{n=o}^{\infty}\left[\delta\left(\omega + \omega_o + \frac{2n\pi}{T_s}\right) + \delta\left(\omega - \omega_o + \frac{2n\pi}{T_s}\right)\right] \quad .$$

As cumbersome as this expression appears, it succinctly demonstrates two important points regarding the effect of the CDS circuit on preamplifier noise. For 1/f noise e_{av} is of the form $e_{f_r}[f_r/f]^{\frac{1}{2}}$, where e_{f_r} is the spot noise measured at a reference frequency f_r. Assuming ω_o to be small compared with the sample rate $2\pi/T_s$ (thus with respect to $2\pi/\Delta t$), $[e_{out}(\omega_o)]_{rms}$ is approximated by

$$\left[e_{out}(\omega_o)\right]_{rms} \sim e_{av}\, \omega\Delta t/\sqrt{2} = e_{f_r}(\pi f_o f_r \Delta t)^{\frac{1}{2}} \quad ,$$

which vanishes as $f_o \to 0$.

The second important point regards the infinite sum in the expression for $[e_{out}]_{rms}$, which describes the aliasing phenomenon due to the sampling operation. If ω_o is not limited to values less than π/T_s (the Nyquist limit), then images fold over into the Nyquist interval $0 \leq \omega < \pi/T_s$ and cause an increase in the rms noise power. These points are illustrated in Figure 4, which shows the product of the CDS transfer function with the aliased noise spectrum for the case $\Delta t = T_s/2$.

Thus, although 1/f noise is suppressed by the CDS circuit, the Johnson noise component is typically increased due to aliasing. Ideally, one would like to band-limit the Johnson noise to the Nyquist frequency by limiting the preamplifier bandwidth. Although this approach eliminates all noise aliasing, it would result in unacceptable signal attenuation because of the short response times imposed by the detector read-out scheme. Assuming the preamplifier frequency response is dominated by a single pole having an effective time constant τ, the rms input referred noise after amplification and CDS is given by

$$V_n = e_n \left(\frac{1}{4\tau}\right)^{\frac{1}{2}} \left\{2\left[1 - \exp\left(\frac{-(t_5 - t_3)}{\tau}\right)\right]\right\}^{\frac{1}{2}} ,$$

where e_n is the input referred noise spectral density ($V/\sqrt{Hz}$) of the preamplifier. From this equation it appears that increasing τ (decreasing bandwidth) and/or decreasing $t_5 - t_3$ (thereby increasing the correlation between samples) is desirable.

However, as τ increases, an increasing fraction of the reset noise remains after clamping, thus reducing the noise reduction properties of the CDS circuit. In view of these limitations, it is suggested in the literature[10] that the use of three to four time constants between reset and clamp, as well as between injection and sample, is optimal. In reality, however, it is anticipated that these intervals will be dictated by recovery time (slew rate) limitations in the preamplifier, which determine its response to the high level reset and

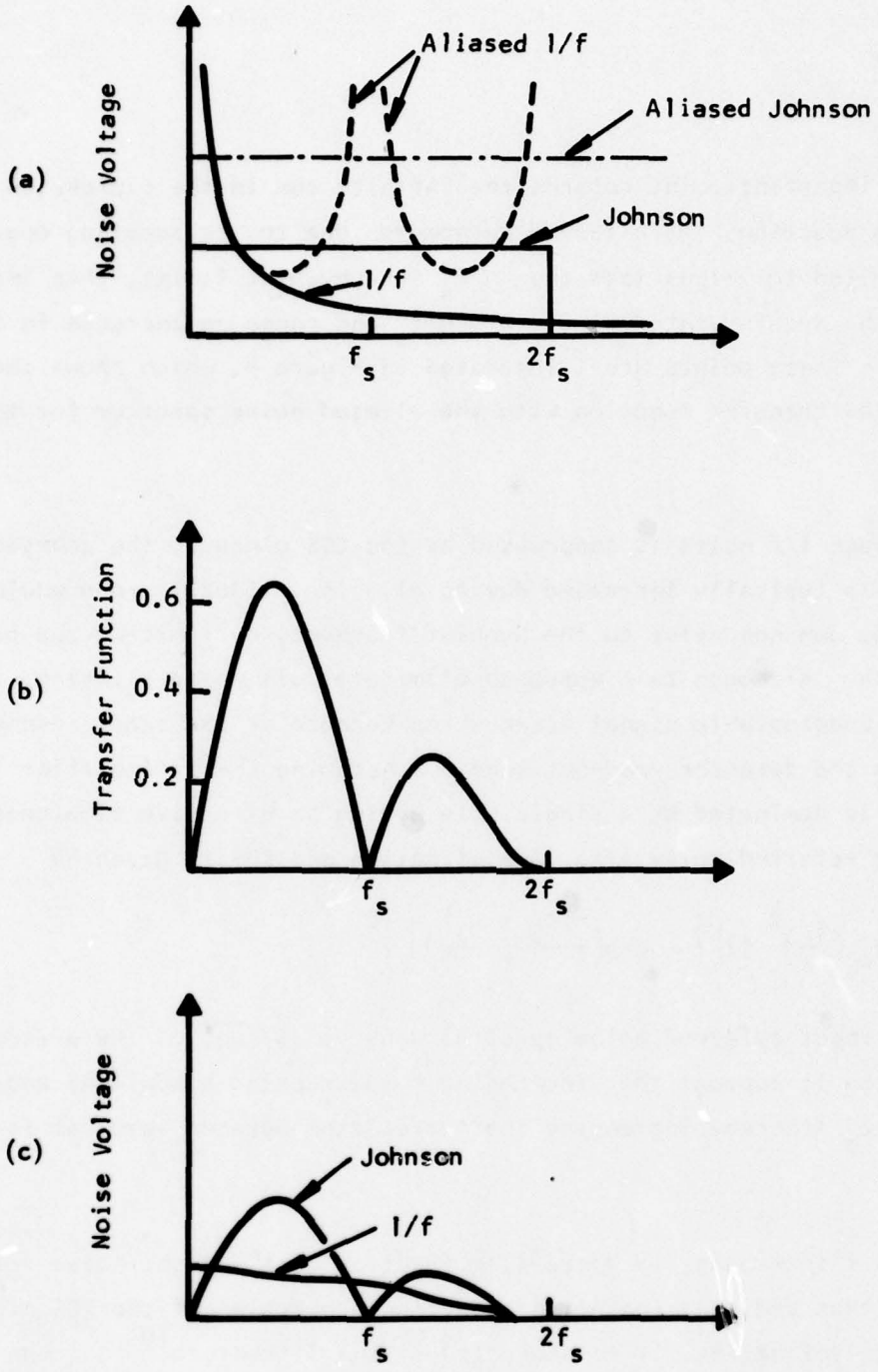


Figure 4 Effect of the CDS Circuit on Noise: (a) Input Noise Spectrum Showing Aliasing Effects, (b) Noise Transfer Function of the CDS, (c) Output Noise Spectrum

inject pulse amplitudes that appear on the detector sense line. Assuming an injection pulse duration of 85 ns and reset, clamp, and sample pulse duration of 50 ns, the total remaining settling time is approximately 440 ns. This requirement must be considered in the design of the preamplifier.

A low noise preamplifier having the configuration shown in Figure 5 was previously designed and fabricated at Texas Instruments for use with a CCD image buffer. Since a CDS circuit was not used in this application, buried channel MOSFETs were employed to improve low frequency noise performance. This device structure effectively moves the current flow away from the "noisy" semiconductor-oxide interface by using a very deep depletion implant. This type of device is therefore characterized by large negative threshold voltages, and its operation is very similar to that of a junction FET.

As mentioned previously, the surface channel mechanism is caused by surface state trapping. In the buried channel MOSFET, however, the low frequency noise mechanism can be related to bulk phenomena, since the conducting channel has been moved away from the surface to the bulk region. More precisely, the low frequency noise mechanism in the buried channel MOSFET can be associated with generation-recombination (g-r) centers within the bulk. Although considerable effort has been devoted to the theory of low frequency noise mechanisms in surface channel MOSFETs, detailed theoretical considerations have not been completely developed for low frequency buried channel devices.

The preamplifier design goals included a gain of 75 with an equivalent Johnson noise component of 4 $nV/\sqrt{Hz}$ and a low frequency noise corner (low frequency noise equal to Johnson noise) at 1 kHz.

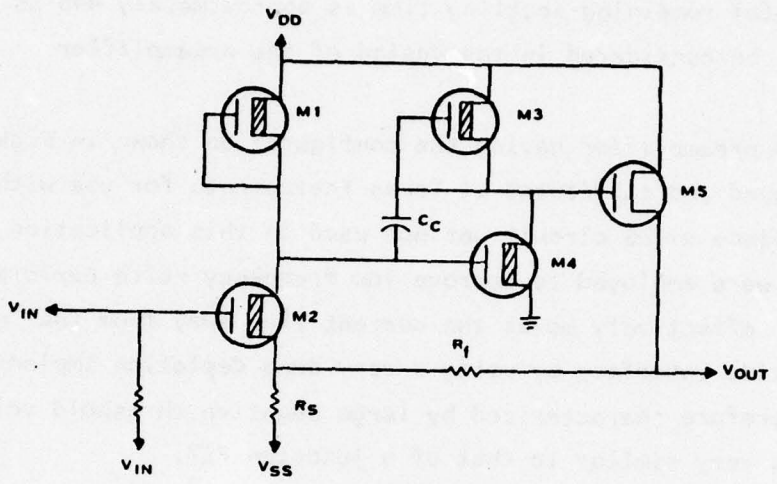


Figure 5 Buried Channel Low-Noise MOS Preamplifier

Typical 1/f corner frequencies for surface channel devices are in the range of 10 kHz to 1 MHz. This design employs two casaded buried channel inverter stages with depletion-type active loads. A surface channel output buffer drives the output load and provides series feedback to the first stage. The input device, M2 is a large interdigitated buried channel structure with noise characteristics determining the overall preamplifier noise performance, since significant gain occurs in the first stage. The device was designed to have a theoretical white noise of 4 nV/$\sqrt{Hz}$ and a low frequency corner of 1 kHz with a W/L ratio of 300 and I_D of 1 mA. The load device of the first stage, M1, is also a buried channel structure with the gate tied to the source, providing a high series resistance typical of depletion load devices. The open loop of this stage is approximately 40.

The second amplifier stage has a design noise of 6 nV/$\sqrt{Hz}$; thus, when referred to the input of the preamplifier, it is a negligible contributor to the total noise. The second inverter gain stage, consisting of M3 with a W/L ratio of 0.2 and M4 with a W/L ratio of 10, provides additional open loop gain and, in conjunction with C_C, provides internal closed loop frequency compensation and bandwidth control. The final stage of the preamplifier is a surface channel source-follower stage that buffers the amplifier output stage for the output load and feedback and reduces the power dissipation in the feedback network. In addition to stabilizing the ac characteristics, the feedback arrangement also stabilizes dc characteristics within the loop, which is particularly important in terms of MOSFET threshold voltage variations. Critical bias voltages must still be supplied at the gate of M2, and the V_{ss} supply must be well regulated and "quiet." To achieve proper operation of the large W/L MOSFETs, substrate bias must be applied. The design value of substrate voltage is -5.0 V.

The feedback resistors, R_f and R_s, are implanted structures fabricated with the buried channel ion implant. Sheet resistivities are on the order of 5 kΩ/square and provide adequate linearity for this application. The closed loop

gain is dependent only on the ratio of these resistances, and absolute values are noncritical if adequate bias can be maintained at the source of M2. A computer-aided design dc analysis program showed linear operation over a ±2 V range at the output.

The measured noise characteristics of the preamplifier are shown in Figure 6. The white noise component is somewhat larger than predicted, an effect that has been identified with the interdigitated geometry of the input device.[11] In addition, the low frequency corner is considerably higher than predicted, and this has been attributed mainly to the surface channel source-follower transistor M5. Based on the experience obtained in the design and analysis of the buried channel preamplifier configuration of Figure 5, a surface channel version of the circuit was selected for use on the silicon processor chip.

The circuit diagram for the low noise preamplifier is shown in Figure 7, which also shows the most important parasitic and compensation capacitances. Note that the output signal is now taken directly from the second stage, thereby eliminating gain degradation in the source-follower, which is employed only to buffer the feedback circuit. Although load resistors are indicated in the figure for the purpose of the ensuing calculations, it is assumed that depletion mode transistors will be employed as load devices and for the feedback divider.

Using simplified circuit models for M1, M2, and M3 (i.e., $I_D = g_m V_{GS}$), the low frequency small signal transfer function is given by

$$A_{VCL} = \frac{A_{V1} A_{V2}}{1 + \alpha A_{V1} A_{V2} A_{V3}} \quad ,$$

where A_{V1}, A_{V2}, and A_{V3} are the open loop voltage gains for each stage given by:

$$A_{V1} = -g_{m1} R_{L1} \Big/ \left[1 + \frac{g_{m1} R_s (1 + g_{m3} R_f)}{1 + g_{m3} (R_f + R_s)}\right] \quad ,$$

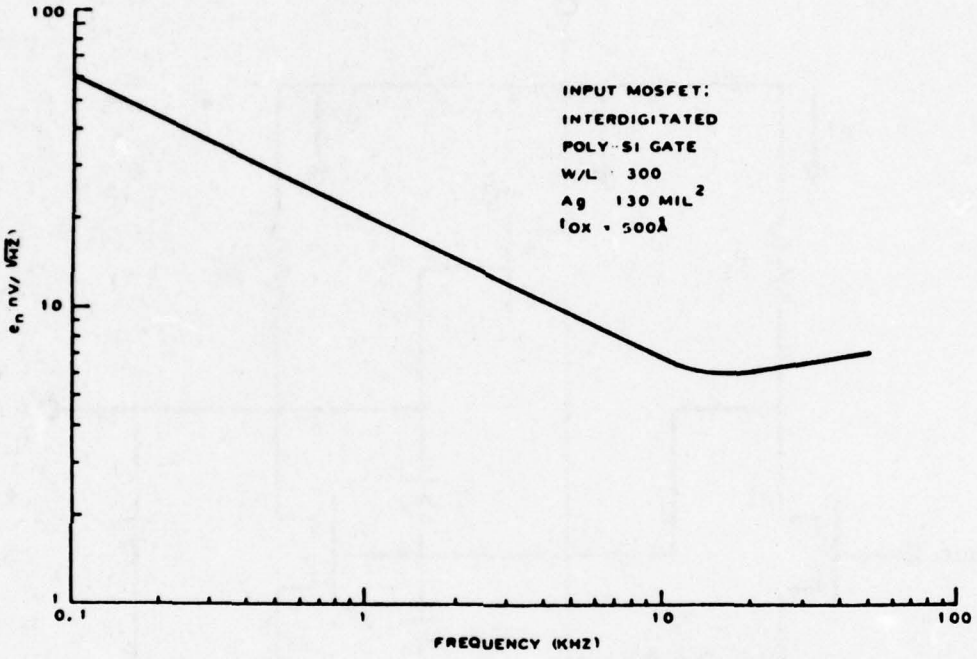


Figure 6 Buried Channel MOS Preamplifier Noise Characteristic

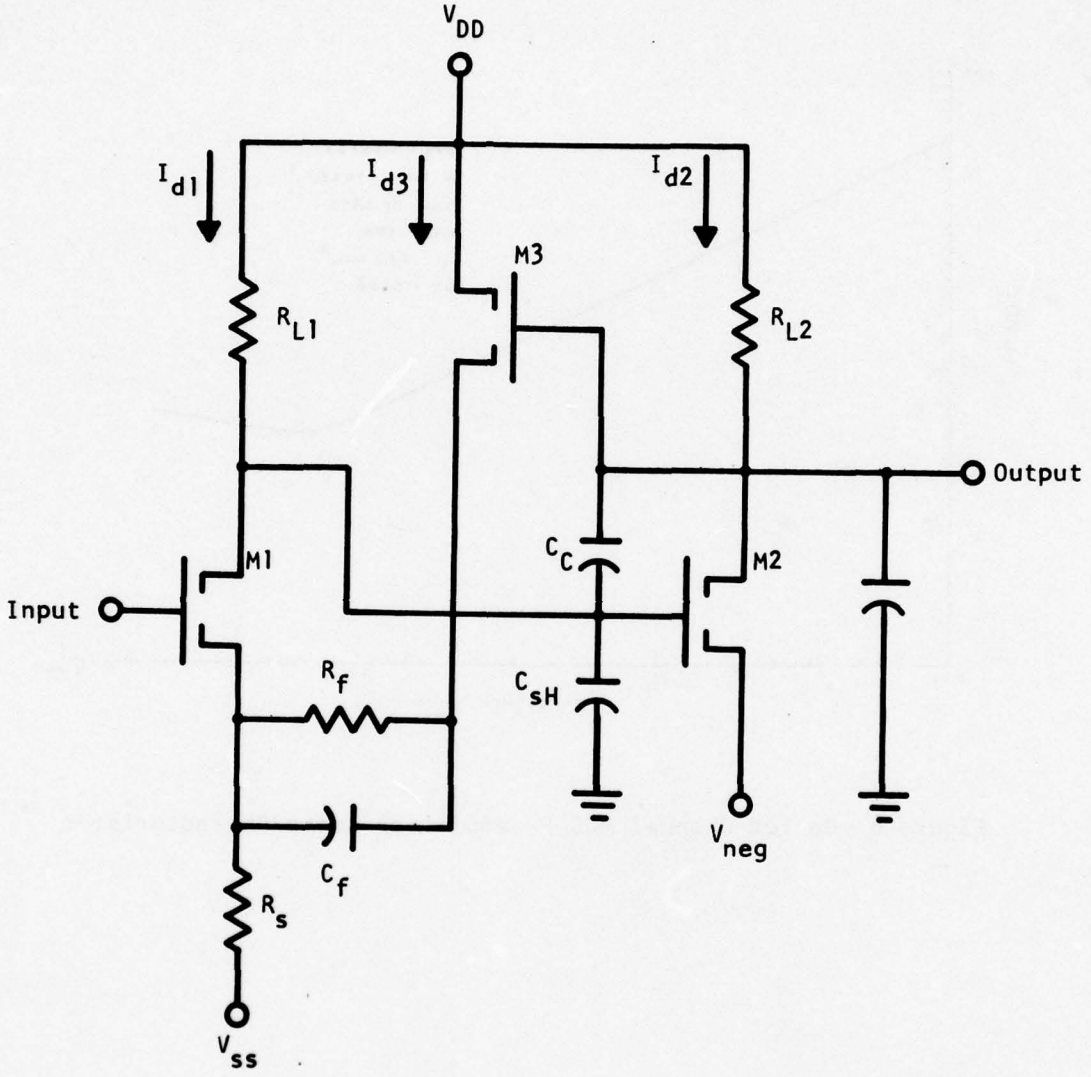


Figure 7 Schematic Diagram of the Feedback Amplifier

$$A_{V2} = -g_{m2} R_{L2} \quad ,$$

$$A_{V3} = \frac{g_{m3} (R_f + R_s)}{1 + g_{m3} (R_f + R_s)} \quad ,$$

and α is the feedback divider ratio $\alpha = R_s/(R_s + R_f)$. Assuming that the low frequency open loop gain $A_{V1} A_{V2}$ is much larger than $1/\alpha$, the high frequency transfer function is approximately

$$A_{VCL}(s) = \frac{A_{VOL}(s)}{1 + A_{VFB}(s)} \quad .$$

$A_{VOL}(s)$ is the open loop gain and $A_{VFB}(s)$ is the gain in the feedback loop:

$$A_{VOL}(s) = \frac{-g_{m1}'(s - g_{m2}/C_C)}{sC^*(s + g_{m2}/C^*)} \quad ,$$

$$A_{VFB}(s) = \frac{-\alpha R_f C_f g_{m1}'(s - g_{m2}/C_C)(s + 1/R_f C_f)}{sC^*(s + g_{m2}/C^*)} \quad ,$$

where $C^* = C_{sH} + C_L + C_{sH}C_L/C_C$ and g_{m1}' is the effective value of g_{m1}, which is reduced by the source-coupled feedback circuit

$$g_{m1}' = g_{m1} \quad 1 + \frac{g_{m1} R_s (1 + g_{m3} R_f)}{1 + g_{m3}(R_f + R_s)} \quad .$$

The small signal bandwidth of the preamplifier can be obtained by comparing $A_{VCL}(s)$ with the low frequency value A_{VCL} obtained earlier. The stability of the preamplifier circuit can be analyzed using the feedback transfer function $A_{VFB}(s)$, which must satisfy

$$-\pi < \angle A_{VFB} < \pi \text{ for } A_{VFB} \geq 1 \quad .$$

In practice, the preceding equations are used in conjunction with dc device models to perform a quick evaluation of gain, bandwidth, and stability for a particular design. Complete characterization of the dc, ac, and transient performance of a preamplifier design was accomplished using a computer simulation program (SPICE). This program utilizes device models having parameters that are experimentally determined using test transistors fabricated with the CCD/NMOS process that will be employed for fabrication of the signal processor chip.

The resulting circuit configuration for the preamplifier is shown in Figure 8, which indicates device W/L ratios, nominal node voltages, and branch currents. Performance specifications as predicted by SPICE simulation are listed in Table 2 along with those dictated by system requirements. The total input capacitance, C_T, is predicted to be approximately 11 pF (including strays), resulting in an input referred noise voltage of 3.8 μV rms. The preamplifier Johnson noise density requirement is then 1.9 $nV/\sqrt{Hz}$, based on the 4.2 MHz preamplifier bandwidth. The predicted noise performance listed in the table is indicative of the result of the key trade-offs among noise performance, power dissipation, and silicon area constraints.

The primary noise sources in the preamplifier are M2 and R_s. If the value of R_s is decreased in an attempt to decrease its noise contribution, the drain current in M3, and, therefore, the power dissipated, must increase in order to maintain the output swing required to accommodate ±100 mV threshold variations in M2. Thus, in the final design R_s and M2 contribute equally to the overall preamplifier noise performance.

The voltage gain of the first stage is 5.6 and results in an input capacitance of 1.2 pF due to Miller multiplication of the gate-drain overlap capacitance. The gate-source capacitance is negligible because of the source-coupled feedback technique. The value of the compensation capacitor, C_C, was determined from SPICE analysis of the transient response of the preamplifier circuit to

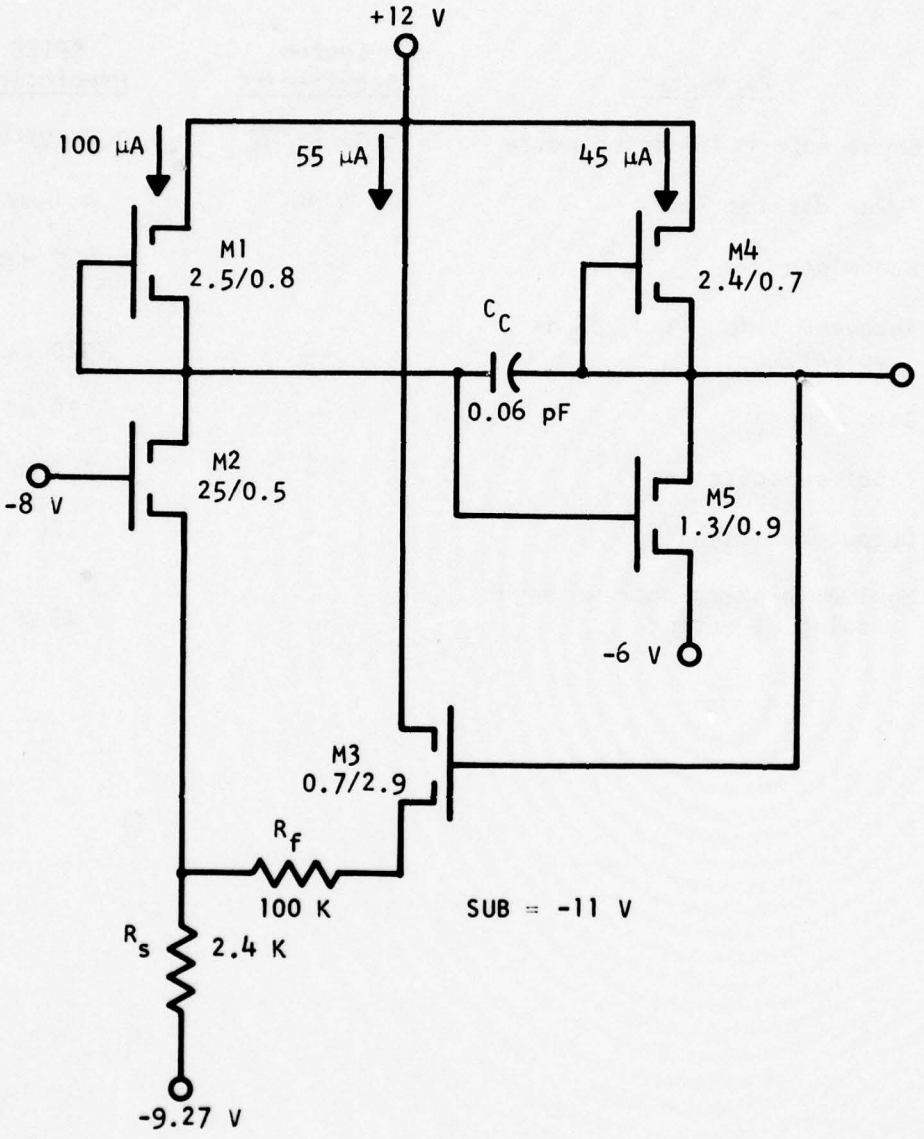


Figure 8 Schematic Diagram of the Low-Noise Preamplifier

Table 2

Preamplifier Performance Specifications

Parameter	System Requirement	SPICE Prediction
Input referred Johnson noise	1.9 nV/$\sqrt{Hz}$	3.7 nV/$\sqrt{Hz}$
Power dissipation	4 mW	4.1 mW
Bandwidth	--	4.2 MHz
Recovery time (+3 V, 85 ns pulse)	--	320 μs
Gain	--	30 dB
Input capacitance	--	1.2 pF
Output resistance	--	120 K
Maximum peak-to-peak voltage swing at output	--	±5 V

reset and injection pulse waveforms. A value of 0.06 pF and an estimated load capacitance of 0.4 pF resulted in the 4.2 MHz small signal bandwidth. The transient due to the reset pulse was predicted to settle out in 120 ns, while that due to the injection pulse requires approximately 320 ns.

The schematic diagram of the CDS circuit appears in Figure 9. One key design consideration is the bandwidth of the source-follower buffer stages, which must be sufficient to allow the clamp and sample operations to occur with sufficient accuracy in the intervals allowed. The bandwidth of the clamp buffer stage is determined by the charging and discharging of C_{SH}, while the bandwidth of the sample-and-hold buffer stage is determined by similar consideration of the TDI circuit input capacitance, C_{TDI}. The gates of depletion load devices M8 and M11 are controlled externally by V_{LG} to allow optimization of the bandwidths.

Another important design consideration is the noise introduced by the CDS circuit. Due to the multiple sampling operations involved, the most convenient point at which a comparison of noise sources can be made is the formation of the signal charge packet in the TDI input circuit. Thus, although detailed consideration of the TDI structure is delayed for a later section, the noise and sampling properties of the TDI input circuit will be discussed here.

The TDI input circuit will operate in the "fill and spill" mode, in which a receiving well beneath an input gate (corresponding to C_{TDI} in Figure 9) is initially completely filled, then emptied to a level dependent on the relative potentials between the signal on the input gate, V_{sig}, and an intermediate gate which is maintained at a reference dc level, V_{ref}. This results in the formation of a charge packet of $(V_{sig} - V_{ref})\ C_{TDI}$ with additional uncertainty given by $\sqrt{kTC_{TDI}}$ due to the charge "spilling" process. Expressed as an uncertainty on V_{sig}, this additional noise component is $\sqrt{kT/C_{TDI}}$.

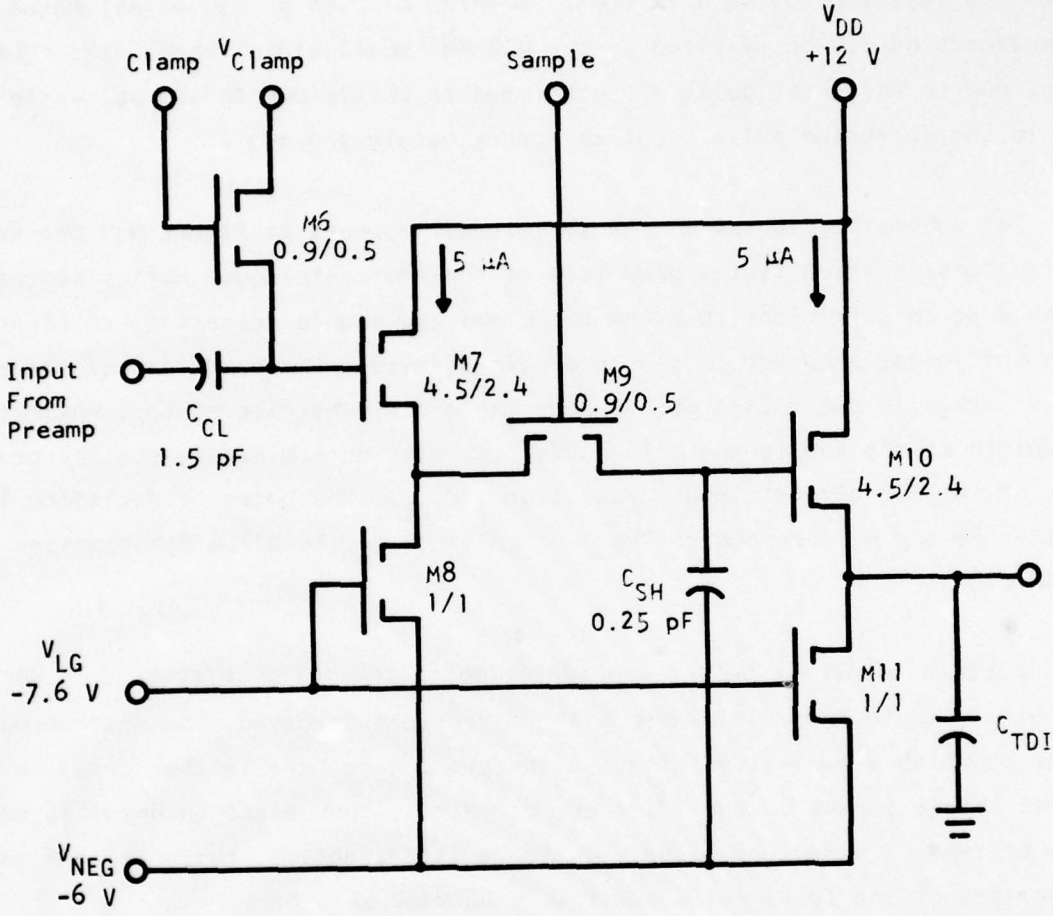


Figure 9 Schematic Diagram of the CDS Circuit

The input referred Johnson noise due to the preamplifier, $(e_{nJ})_{preamp}$, experiences the gain of all three amplifiers and is aliased in the CDS sample operation. The second sampling operation in the TDI input circuit does not measurably affect this component further, due to the low-pass filtering effect of the CDS sample-and-hold. At the TDI input, the rms value of the preamplifier Johnson noise component is

$$e_{n1} = A_{preamp}\, A_{CL}\, A_{SH}\, [2BW/f_s]^{\frac{1}{2}}\, (e_{nJ})_{preamp},$$

where A_{preamp} is the voltage gain of the preamplifier ($A_{preamp} = 34$); A_{CL} and A_{SH} are the voltage gains in the clamp and sample source-follower buffers, respectively; ($A_{CL} = A_{SH} \sim 1$); BW is the preamplifier small signal bandwidth; and f_s is the sample rate. Inserting the appropriate values [BW = 4.2 MHz, f_s = 1.48 MHz, $(e_{nJ})_{preamp}$ = 7.6 μV rms] results in e_{n1} = 614 μV rms. The quadrature sum of all other noise sources must be substantially smaller than e_{n1}.

The Johnson noise generated in the clamp buffer stage is aliased by the sample operation. The noise generated in the clamp circuit, referred to the TDI input, is then

$$e_{nCL} = \sqrt{kT} \left[\frac{1}{C_{CL}} + \frac{16\ BW_{CL}^{\,2}}{3 f_s\ g_{m7}} \right]^{\frac{1}{2}},$$

where BW_{CL} is the bandwidth of the clamp buffer stage and g_{m7} is the transconductance of device M7, which is given by $(2K\ I_D\ W/L)^{\frac{1}{2}}$. SPICE simulation indicates that BW_{CL} is approximately 10 MHz, and g_{m7} is calculated to be approximately 9.7 μmho. The calculated value is then e_{nCL} = 27 μV.

Johnson noise generated in the sample-and-hold buffer is aliased by the sampling effect of the TDI input circuit. The noise generated in the sample-and-hold circuit is then

$$e_{nSH} = \sqrt{kT}\left[\frac{1}{C_{SH}} + \frac{16\ BW_{SH}^{2}}{3f_s\ g_{m10}}\right]^{\frac{1}{2}} ,$$

where BW_{SH} is the bandwidth of the sample-and-hold buffer stage and is the same as for the clamp buffer; and g_{m10} is the transconductance of device M10, which, although a depletion mode device in order to eliminate large dc offsets through the CDS circuit, exhibits approximately the same parameters as device M7. The resulting calculation gives $e_{nSH} = 65\ \mu V$ rms.

The predicted value of C_{TDI} is 0.044 pF, based on the geometry of the input circuit. The voltage equivalent uncertainty due to C_{TDI} is $e_{n_{TDI}} = 156\ \mu V$ rms. The quadrature sum of CDS and TDI related noise sources is then 171 μV rms and results in a total noise voltage of 637 μV rms, which is only 4% greater than the preamplifier Johnson noise component.

An additional consideration pertinent to the noise performance of the CDS circuit involves the 1/f noise generated in M7 and M10, which is not attenuated by operation of the CDS circuit. The 1/f noise component is approximately given by

$$\overline{e_n^{2}}(1/f) = (q/C_{ox})^{2}\ \frac{N_{ss}}{80\ fWL}\ F(V_{GS}) ,$$

where C_{ox} is the gate oxide capacitance (0.22 pF/mil^2 for the CCD/NMOS process); N_{ss} is the surface state density (typically $\sim 10^{10}/cm^2$); and $F(V_{GS})$ is a gate-source bias factor, which is on the order of unity. As can be seen, the noise power is inversely proportional to gate area, and devices M7 and M10 were designed with the largest gate area deemed practical.

Evaluating the above expression results in

$$e_n(1/f) \sim \frac{6.4}{\sqrt{f}}\ \mu V/\sqrt{Hz} .$$

Since aliasing does not affect 1/f noise (it is, by definition, band-limited), we can multiply this result by $\sqrt{2}$ to obtain the combined 1/f noise due to M7 and M10 and compare this to the preamplifier Johnson noise component referred to the CDS output. The resulting 1/f corner is calculated to be at approximately 100 Hz.

Operation of the CDS circuit was simulated using the SPICE program, which indicated satisfactory performance with 50 ns clamp and sample pulse widths.

Figure 10 is a photomicrograph of a portion of the completed processor bar showing the details of the signal conditioning circuit. Each of the components shown in Figures 8 and 9 is labeled for identification. Note that the structures have been positioned in a mirror-image configuration that simplifies interconnection. The bus lines running horizontally at the top and bottom of the picture carry clock waveforms for the TDI, ac couple/dc restore, and multiplexer structures. The bus lines running between the two circuits are predominantly dc supply lines. Considerable attention was devoted to minimizing crossovers between clock lines and signal or dc supply lines throughout the chip.

B. CCD Time-Delay-and-Integration (TDI)

The function of the TDI is to increase the signal-to-noise of the detector output by integrating each pixel over a number of samples. In a staring sensor this can be accomplished by a simple integration process applied to each detector element. In this case, however, the ultimate dynamic range is limited by detector responsivity variations rather than the achievable thermal noise level. In the case of a scanned two-dimensional array, consecutive samples from consecutive detector elements must be delayed before integrating to account for movement of the scene relative to the array.

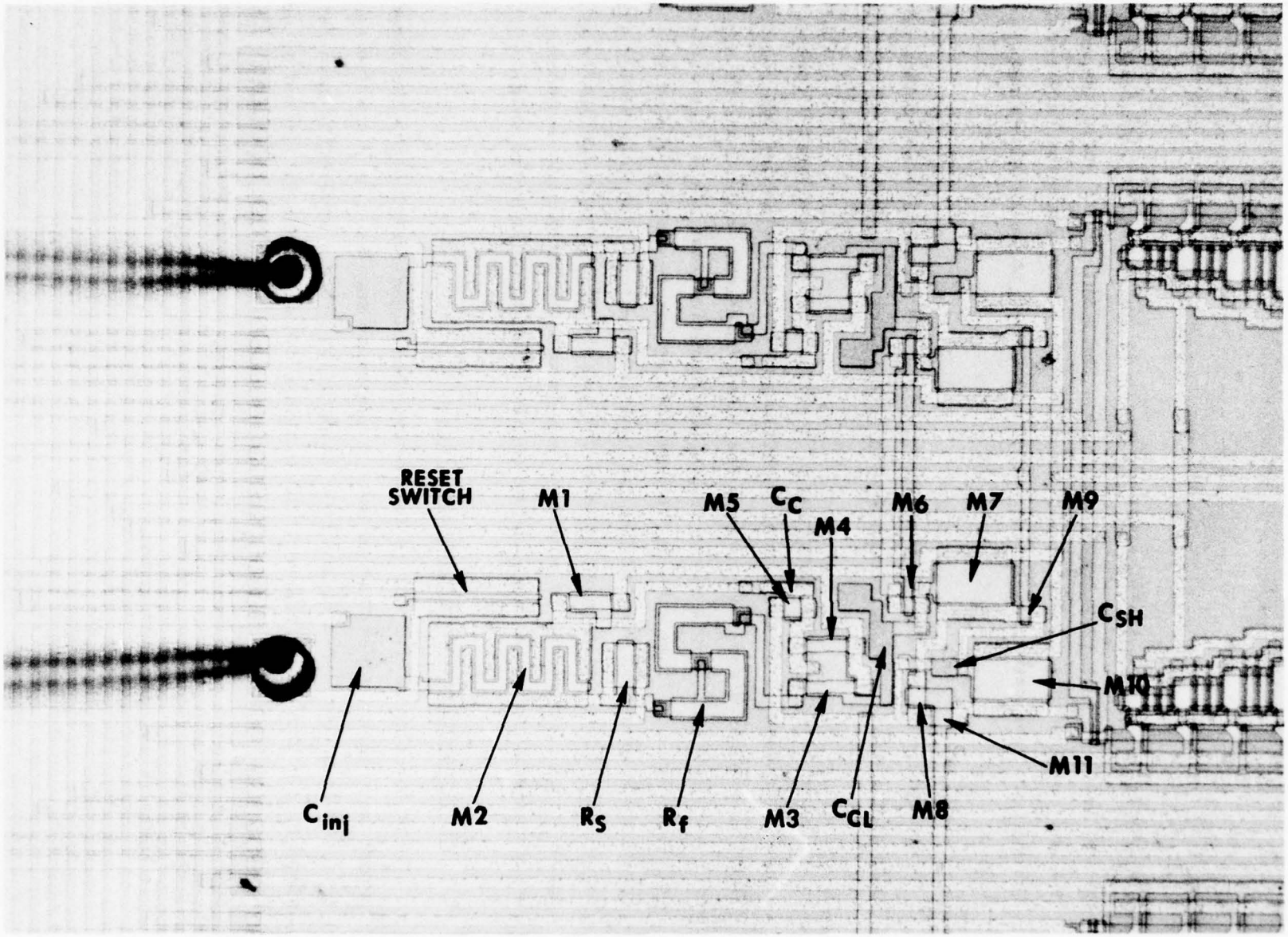


Figure 10 Photomicrograph of the Processor Bar Showing Details of the Preamplifier and CDS Circuits

This operation is illustrated in Figure 11, which demonstrates the response of a single column of detectors (say, from a 4X M array) to a test image consisting of two point sources, S_1 and S_2. The detector elements are connected in parallel to the four inputs of a CCD summing register. During the time-delay phase, all charge in the register is transferred by one cell toward the output node. During the integration phase, the signal charge due to each consecutive detector element is transferred into consecutive register cells. Thus, as the point source image, S_1, is scanned by the detector column, four samples of the image are acquired and integrated into a single output sample, which is proportional to

$$\sum_{n=1}^{4} (r_n S_1 + N_n) \quad ,$$

where r_n is the responsivity of the n^{th} detector cell and N_n is the noise introduced on the n^{th} sample. The signal component of the output sample is $4\bar{r}S_1$, where $\bar{r}$ is the average responsivity $(r_1 + r_2 + r_3 + r_4)/4$. Assuming all noise contributions are due to the same stochastic process, the noise component of the output sample is $[4N_n^2]^{\frac{1}{2}}$. Thus, the effect of the TDI is to improve the signal-to-noise ratio by a factor of $\sqrt{n}$; in addition, it provides an averaging of detector responsivities that results in a performance margin against the failure of a few detector elements.

CCD structures have been designed to delay and add the parallel signals from a number of serially scanned detectors.[12,13] In these applications (similar to the situation depicted in Figure 11) the detector signals are continually loaded in parallel (via individual CCD input circuits) into a CCD register as the register is clocked. Since the CID array multiplexes the detector signals in a TDI column, the TDI structure must incorporate a demultiplexer to perform the serial-parallel conversion required to permit parallel entry of the detector signals into the summing register. Over-sampling the detectors further complicates the design.

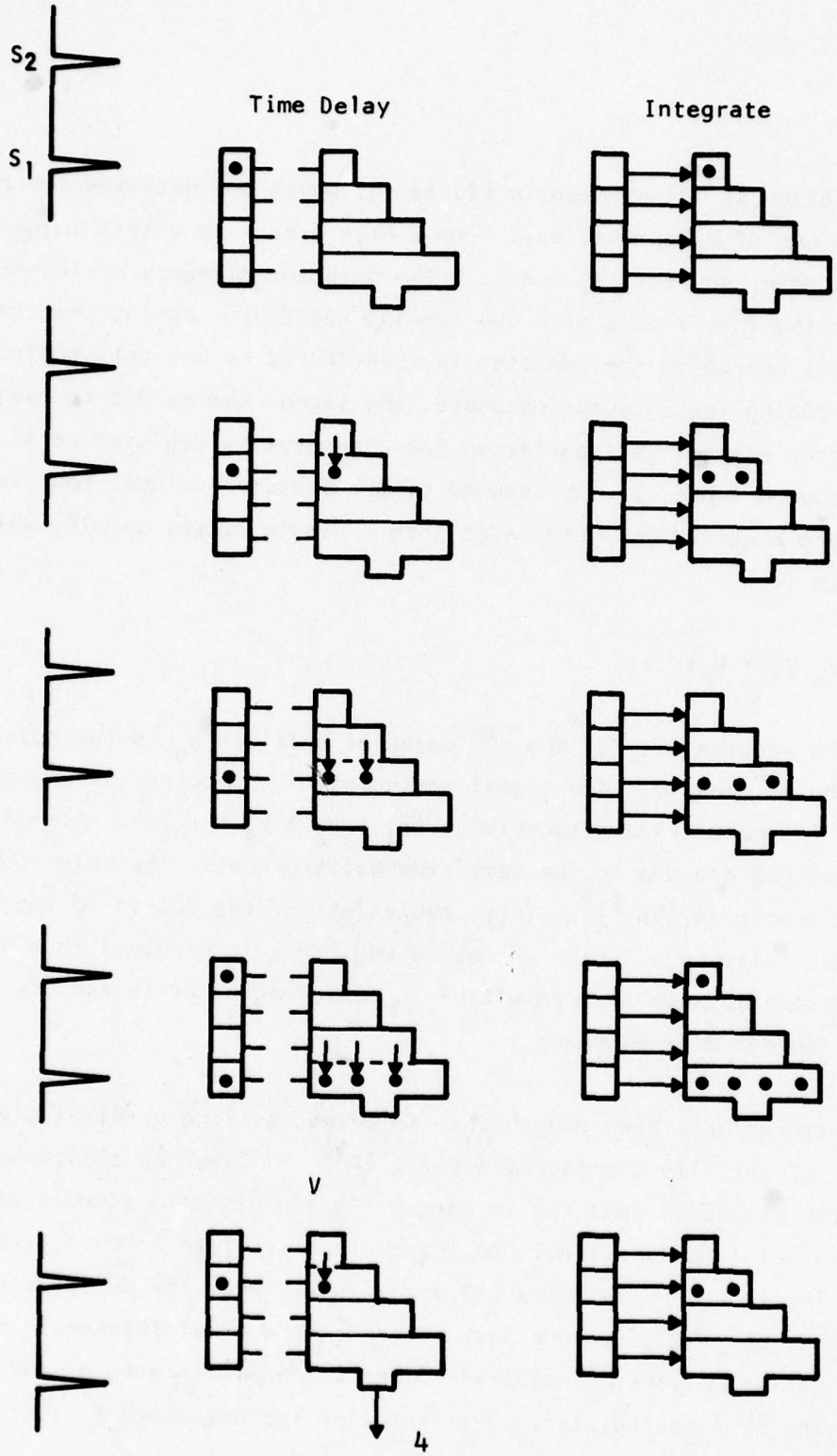


Figure 11 Response of a Four-Stage TDI to Point Images S_1 and S_2

The scan and sample rates are interrelated such that three samples are acquired in the time interval required for a point source to be scanned a distance corresponding to the center-to-center spacing between detector elements in the scan direction. (The detector active area is, by necessity, smaller than the element area, and the dwell time -- defined as the interval required for a point source to be scanned across the active area -- results in the $2\frac{1}{4}$ samples/dwell time specification.) Thus, 48 samples are acquired from each detector in the time interval required for the point source to be scanned across the 16-element TDI column, and the TDI summing register must include 48 individual storage locations. Including the self-multiplexed format of the CID detector read-out scheme, the CCD TDI structure must consist of a 16-stage analog demultiplexer coupled to a 48-stage summing register.

Figure 12 is a sketch of the resulting CCD structure, illustrating the 3:1 interleave requirement (three summing register stages: one demultiplexer stage) and the use of "floating diffusion" stages to accommodate the differences in cell spacing. Both CCD registers are two-phase devices employing ion implanted potential wells to form the charge storage regions. Figure 13 illustrates operation of the floating diffusion stages in the demultiplexer. In Figure 13(a) a signal charge packet, Q_s, is shown stored in a potential well under the ϕ_1 electrode with both ϕ_1 and ϕ_2 clocks at a low potential ("off"). When ϕ_2 is turned "on" in Figure 13(b), Q_s is transferred onto the floating diffusion. In Figure 13(c) ϕ_2 has been returned to the "off" state, and ϕ_1 is "on," resulting in transfer of Q_s from the floating diffusion into the potential well under the ϕ_1 gate. Finally, in Figure 13(d) the ϕ_1 clock is turned "off," and Q_s is again stored in a ϕ_1 well from which it can be transferred either along the demultiplexer (by repeating the sequence) or into the summing register (via the parallel transfer gate -- into the page in the figure).

The transfer from the floating diffusion into the ϕ_1 well in Figure 13(c) is a "bucket brigade" type charge transfer. The charge transfer efficiency (CTE)

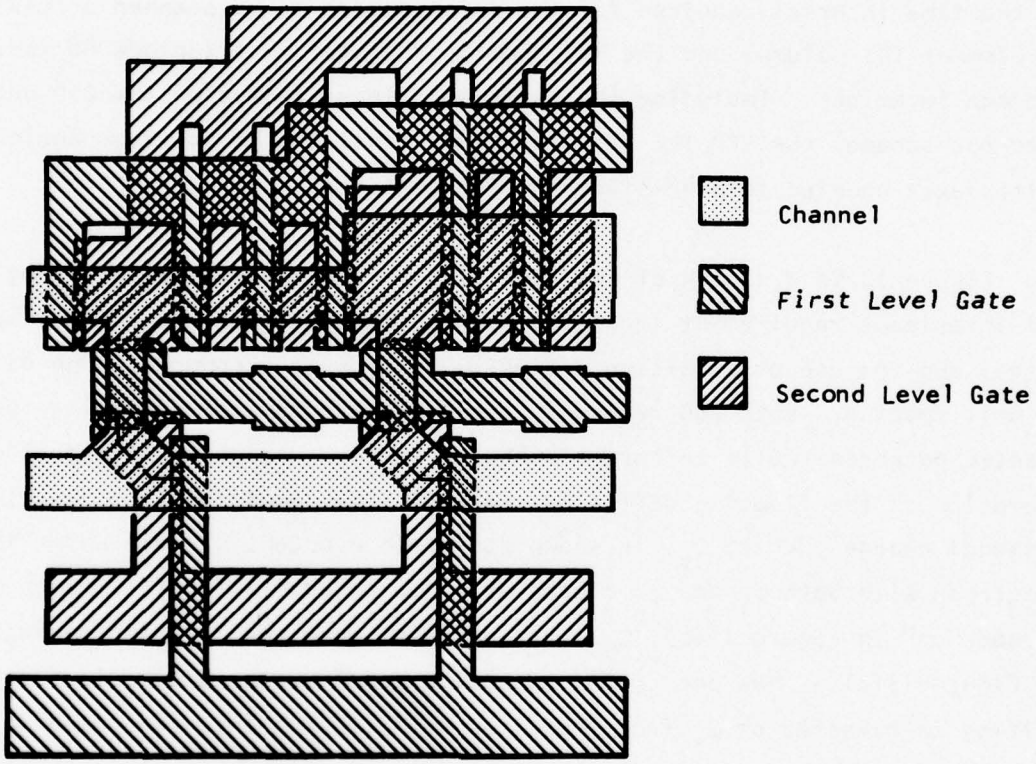


Figure 12 Channel Stop and Polysilicon Gate Levels in the TDI Structure Showing the 3:1 Interleave

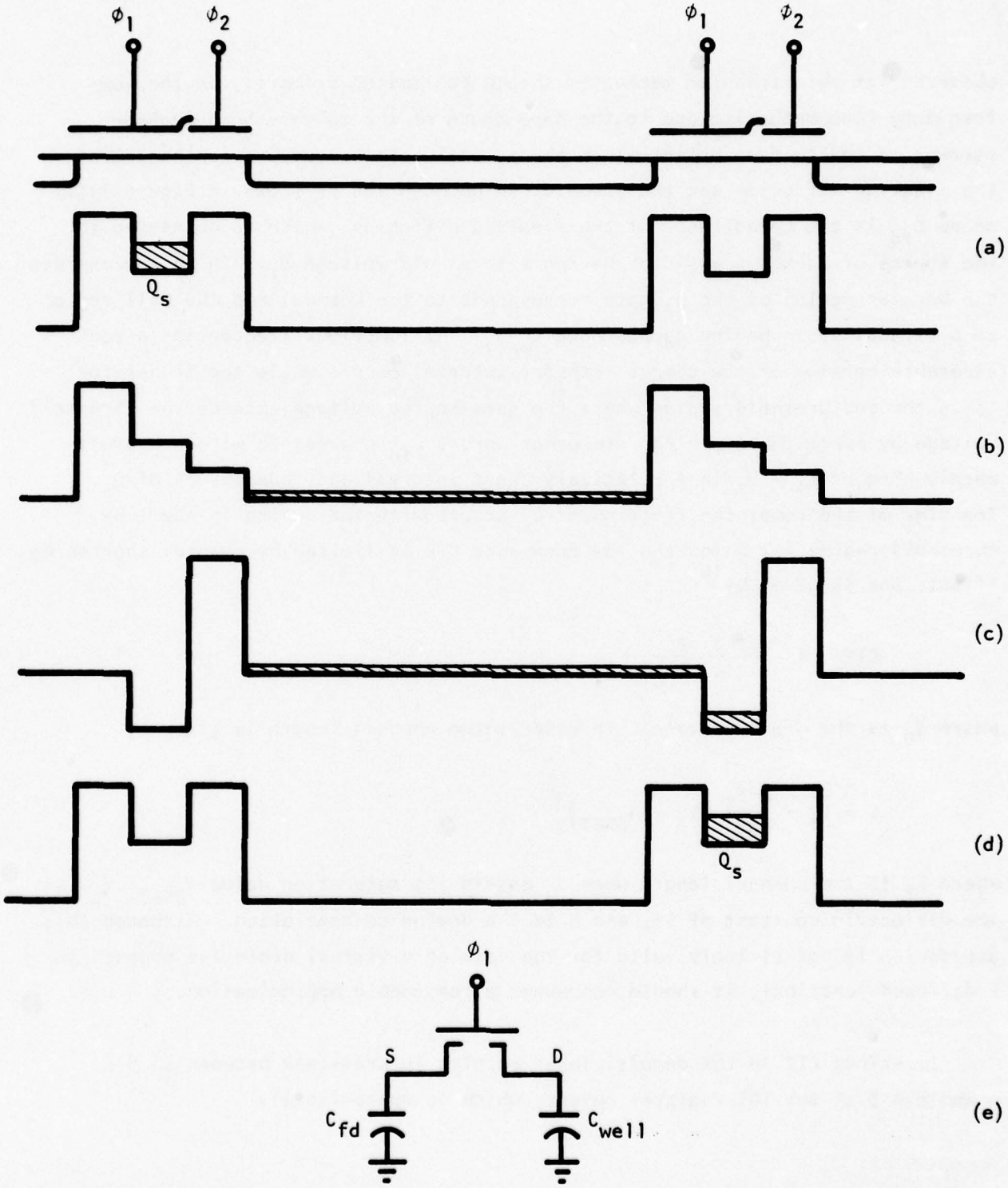


Figure 13 Operation of the Floating Diffusion Stages in the Demultiplexer.
(a) through (d) Operation of the floating diffusion transfer stage.
(e) Equivalent circuit diagram.

observed for this transfer mechanism should be limited primarily by the low frequency loss mechanism due to the dependence of the subthreshold leakage current on the surface potential in the ϕ_1 well. The structure consisting of the floating diffusion and the ϕ_1 gate can be modelled as shown in Figure 13(c) where C_{fd} is the capacitance of the floating diffusion, which is connected to the source of an MOS transistor having a threshold voltage V_T. In this transistor the barrier region of the ϕ_1 gate corresponds to the channel and the well region to a virtual drain having capacitance C_{well}. At low clock frequencies a considerable portion of the charge transfer interval occurs while the transistor is in the subthreshold region where the gate-source voltage exceeds the threshold voltage by approximately kT/q. In other words, C_{fd} charges to within approximately kT/q of $\phi_1 - V_T$ in a relatively short interval and independent of Q_s. Transfer of the remaining fraction of Q_s occurs with the device in the subthreshold regime for which the low frequency CTE is limited by channel shortening effects and is given by[14]

$$CTE = 1 - \frac{kT}{q} \frac{1}{L} \frac{\partial L}{\partial V_D} \quad ,$$

where V_D is the drain voltage. In MOSFETs the channel length is given by

$$L = L_T - \left[\frac{2\epsilon_s}{qN} \left(V_D - V_{DSAT}\right)\right]^{\frac{1}{2}} \quad ,$$

where L_T is the channel length when V_D equals its saturation value V_{DSAT}, ϵ_s is the dielectric constant of Si, and N is the doping concentration. Although this expression is not strictly valid for the case of a virtual drain (as opposed to a diffused junction), it should represent a reasonable approximation.

Imperfect CTE in the demultiplexer results in crosstalk between samples n and n + 3 at the TDI register output, which is approximately

$$\frac{\text{error}}{\text{signal}} = \frac{\sum_{n=1}^{16} (1 - CTE^n)}{\sum_{n=1}^{16} (CTE)^n}$$

Assuming that the crosstalk must be less than 1%, the resulting CTE requirement is 0.999, and the minimum gate length for the ϕ_1 electrode is calculated to be approximately 0.7 mil.

Important noise sources that remain to be considered include the reset noise introduced at the TDI output node and the Johnson and 1/f noise components in the TDI output amplifier. Although a charge gain of approximately 16 is realized through the TDI, output capacitance considerations result in approximately unity peak-to-peak voltage gain. Since the charge gain applied to the input noise is 4, the rms voltage gain applied to the noise is 0.25. Thus, the expected rms noise level at the TDI output node is 159 μV. The total TDI output node capacitance, C_{out}, is predicted to be 0.7 pF, resulting in an rms reset noise given by $[kT/C_{out}]^{\frac{1}{2}}$ and evaluated to be approximately 40 μV. The total output noise level at the source-follower input is 164 μV rms. In addition, it is low-pass filtered by the sin x/x response of the output circuit and is not substantially affected by the sampling operation in the multiplexer input circuit.

The source-follower transistor is predicted to have a g_m of about 7 μmho and a corresponding Johnson noise density of 20 nV/$\sqrt{Hz}$. The source-follower stage bandwidth is predicted to be about 600 kHz; thus, the Johnson noise component will be aliased by the 92.5 kHz sampling in the multiplexer input circuit. The resulting rms noise voltage, including aliasing, is 56 μV, and the total noise voltage at the multiplexer input (assuming unity gain in the source-follower) is 173 μV rms. The 1/f noise generated in the output amplifier (1.8 mil^2 gate area) is approximately $15/f^{\frac{1}{2}}$ μV/$\sqrt{Hz}$. The resulting 1/f corner is calculated to be approximately 250 Hz.

Figure 14 is a photomicrograph of the completed chip showing the TDI structure. Note the spacings between TDI output nodes labeled on the picture.

C. Ac-Couple/Dc-Restore and CCD Multiplexer Circuits

Dc restoration is accomplished by performing a dc clamp via the dc restore switch on the multiplexer input gate, which is capacitively coupled to the TDI output circuit (refer to Figure 1). This operation removes all electronic offsets in the detector and processor circuits and, in addition, removes detector background response nonuniformities if a thermal reference is scanned by the detector array during the clamp.

The primary design consideration for the 24-channel multiplexer is minimization of channel-to-channel dc offsets, which result in a noise component that exhibits a "fixed pattern" temporal distribution in the multiplexer output waveform. These fixed pattern noise components are commonly associated with CCD multiplexers and are typically attributed to MOS threshold voltage variations among the input circuits that perform the voltage-to-charge conversion. The potential equilibration or "fill-and-spill" input technique[15] is the least sensitive of the standard CCD input circuits in this regard, since the signal charge packet is defined by the difference in surface potential between two adjacent CCD electrodes. However, although the absolute value of the threshold voltage of either gate is not involved, the difference between threshold voltages typically causes 20 to 50 mV fixed pattern offsets in CCD multiplexers.[16] A threshold independent input scheme has been described in the literature[17]; however, close examination revealed that it is not compatible with the ac couple/dc restore operation required for the signal processor circuit, since it necessitates dc-restoring the input node once per clock period.

Another alternative that was considered completely eliminates the use of a CCD structure and accomplishes the multiplexing function by sequentially addressing an array of analog MOS switches that are connected to a common output bus line.

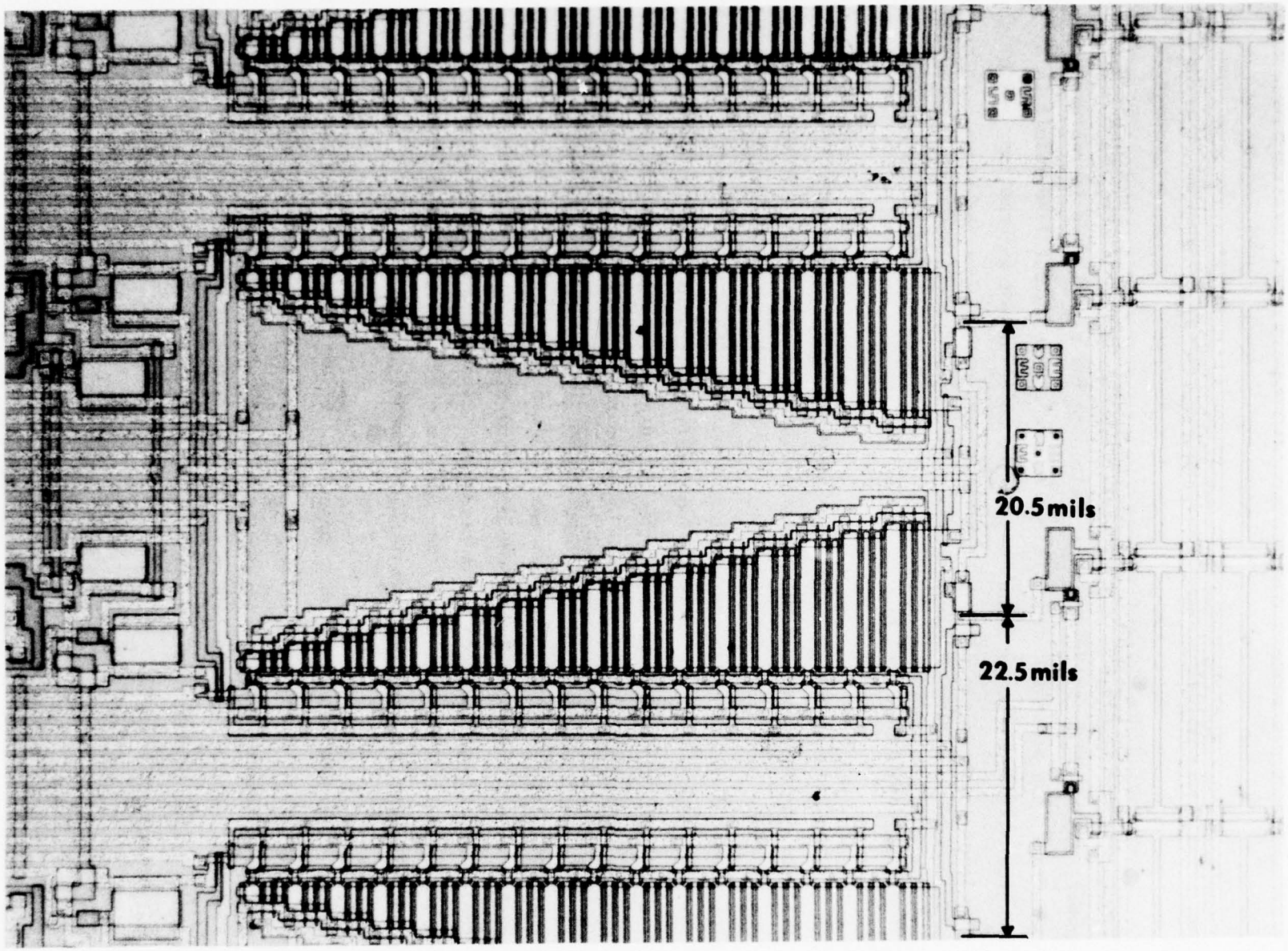


Figure 14 Photomicrograph Showing Details of the TDI Structure and Output Node Spacing

Sequential addressing can be accomplished on the processor chip using a low power, dynamic NMOS shift register. Although the signal node is restored once per frame, the parasitic capacitances to the common output line result in a "charge-mixing" effect and the loss of the dc reference information. As a result of these considerations, the "fill-and-spill" input technique must be employed, and the fixed pattern offsets must be processed out in external signal processing circuitry.

A secondary design consideration involves matching the pitch of the multiplexer to the spacing of the processor channels (the spacing between TDI output nodes indicated in Figure 14). There are two alternatives: (1) fan in TDI signal lines to match the smaller pitch of a CCD structure, or (2) elongate the multiplexer transfer cells, using floating diffusion interconnects (as in the TDI demultiplexer), to match the TDI output node spacing. The decision was made to employ the latter approach based on concerns for matching capacitances of long signal leads and minimizing induced clock noise. In addition, a dual-channel, phase-multiplexed design was utilized that reduces the clock rate in each channel, thereby reducing the potential signal degradation due to low CTE in the floating differsion transfer cells. Since 24 channels are read out in 1/92.5 kHz (1/TDI output rate), the data rate at the multiplexer output is 2.2 MHz, although the transfer rate in each channel is 1.1 MHz.

A two-stage source-follower output buffer amplifier was designed to drive 10 pF external capacitance while maintaining a 10 MHz bandwidth. This amplifier was predicted to exhibit a voltage gain of 0.85 and to dissipate 11 mW. The mismatch between the capacitance of the multiplexer input gate and the capacitance of the output node results in a voltage gain of 0.6 at the multiplexer output node.

The dominant thermal noise sources in the multiplexer are the reset noise in the input and output circuits and the Johnson and 1/f components in the

output amplifier. The multiplexer input well capacitance is 0.2 pF, resulting in an equivalent noise voltage of 73 μV rms which, combined with the noise level calculated in the previous section, yields a total multiplexer input noise voltage of 188 μV. The output node capacitance is predicted to be 0.35 pF and results in a 55 μV rms reset noise component and a total output noise level of 126 μV rms.

The Johnson noise component in the output amplifier is negligible due to the relatively large W/L ratios and drain currents employed. The 1/f component is dominated by the first-stage driver transistor, which has a gate area of 2.25 $mils^2$ and a resulting 1/f component given by $14/f^{\frac{1}{2}}$ $\mu V/\sqrt{Hz}$. Note that the effect of the multiplexer is to reduce the output referred noise density by $1/\sqrt{N}$, where N is the number of channels. The resulting 1/f corner can be expected to increase considerably and is calculated to occur at about 11 kHz. Thus, the 1/f noise performance of the entire processor circuit is expected to be dominated by the component generated in the output buffer amplifier.

Figure 15 is a photomicrograph of a portion of the completed processor bar. It shows details of the ac couple/dc restore, multiplexer, and output buffer amplifier structures.

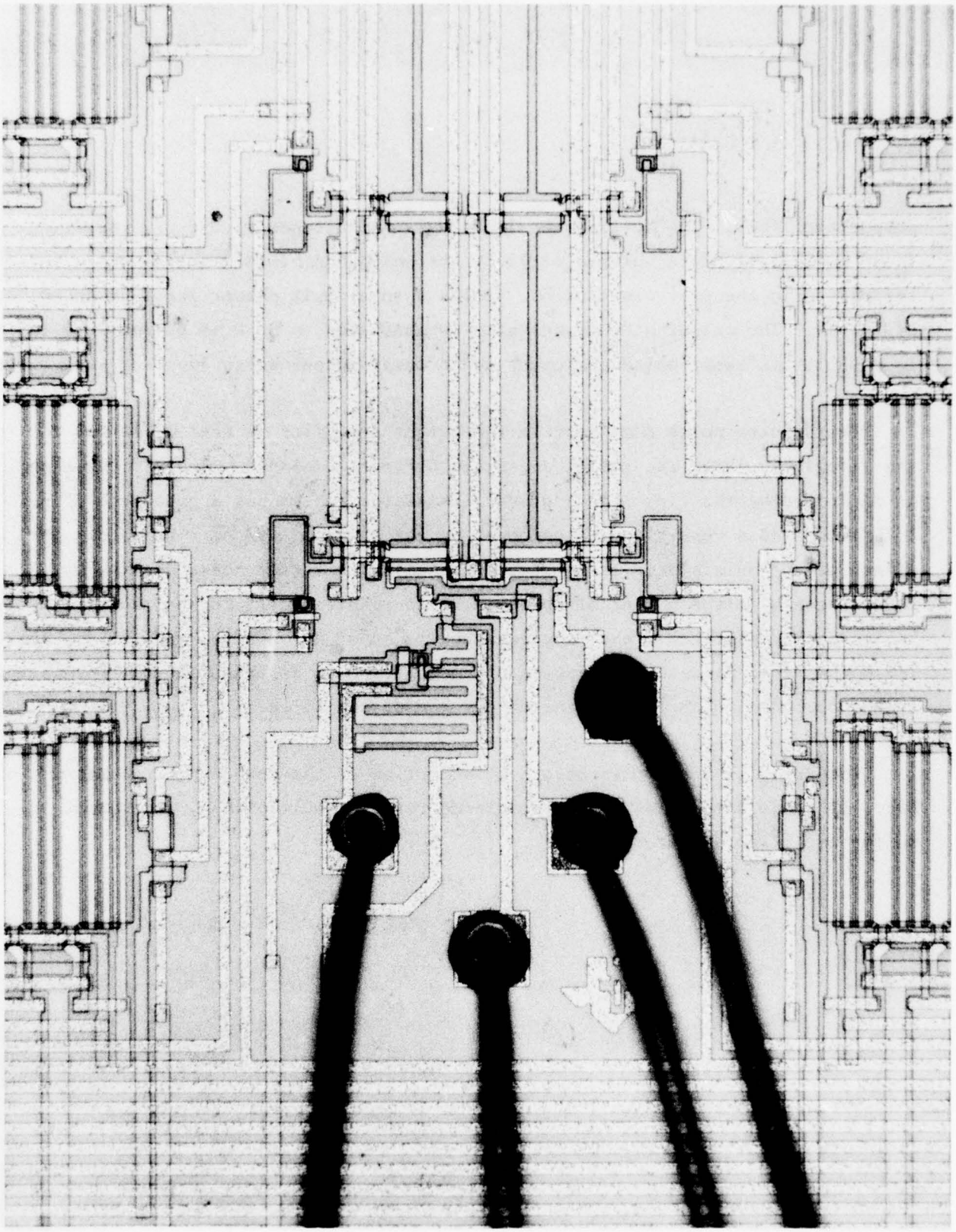


Figure 15 Photomicrograph Showing Multiplexer Output Circuit

SECTION IV
PROCESSOR TESTS

The silicon signal processor chip was fabricated using a double-level, self-aligned polysilicon gate NMOS/CCD process developed at Texas Instruments. A photomicrograph of the completed processor chip appears in Figure 16. In addition to the processor chip, a test chip was designed and fabricated that included each of the major components as a separately bondable test structure. This allows full characterization of each of the component circuits at 77 K with small laboratory liquid nitrogen dewars and considerably less equipment than is required to support operation of the full processor circuit. A photomicrograph of the test chip appears in Figure 17.

In addition to test structures for the preamp, CDS, TDI, multiplexer, and output buffer circuits, a number of test structures were included to allow more complete experimental evaluation of circuit parameters. A second preamp structure was included that features bondable options for input transistors having W/L ratios ranging from 50 to 200 and compensation capacitors having value from 0.06 pF to approximately 3 pF. Another test structure included the preamp, CDS, and TDI circuits, which were interconnected to form a dual channel processor test circuit.

A timing circuit was designed and constructed that provides the numerous clock waveforms required for operation of the processor chip. The circuit was utilized for the tests described in this section and is described in detail in Appendix A. The remainder of this section is devoted to discussion of the data resulting from evaluation of the major test circuits.

A. Preamplifier Tests

The preamplifier test circuit is identical to that used in the processor chip, except that the compensation capacitor must be bonded into the circuit,

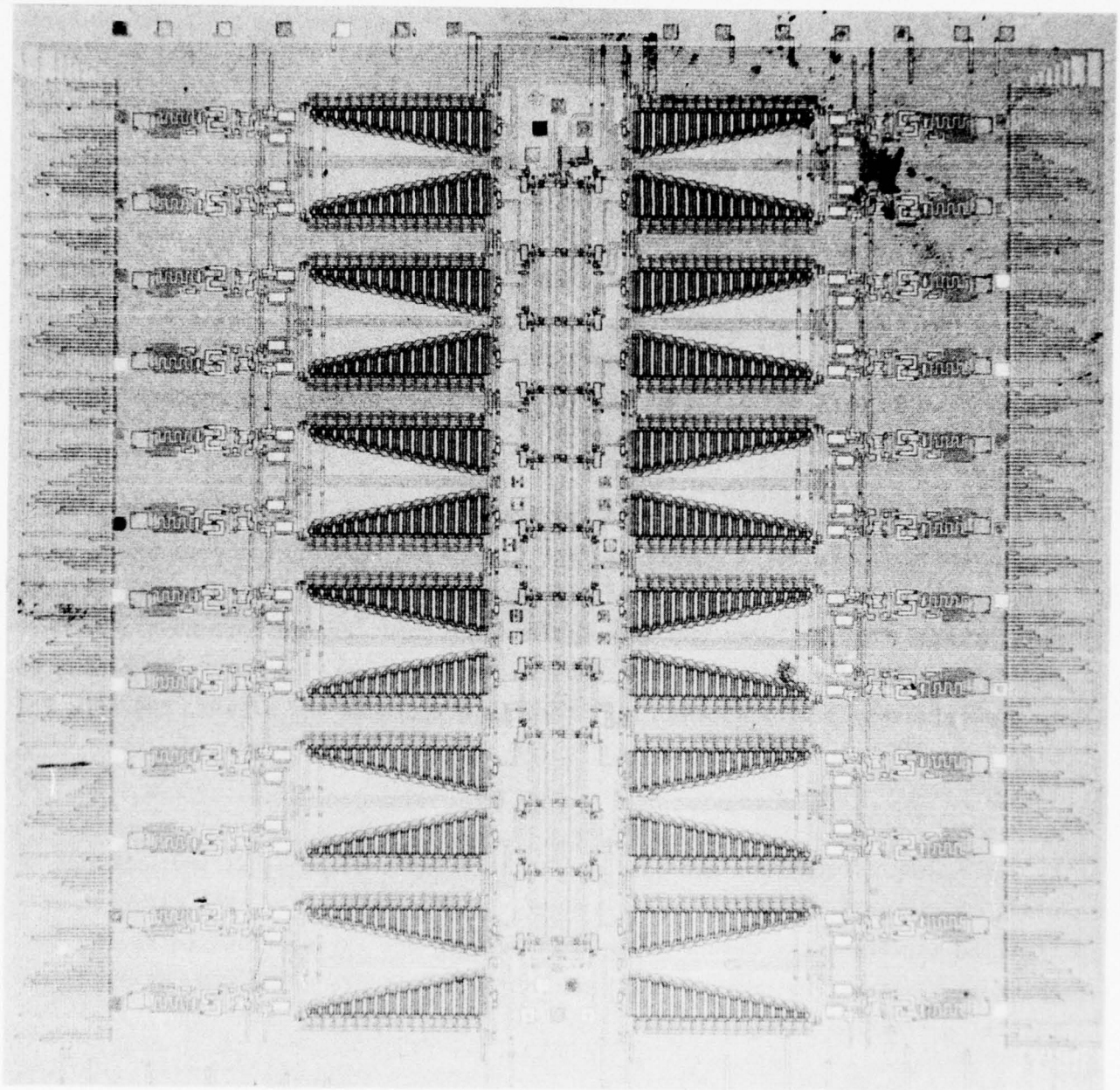


Figure 16 Silicon Focal Plane Processor

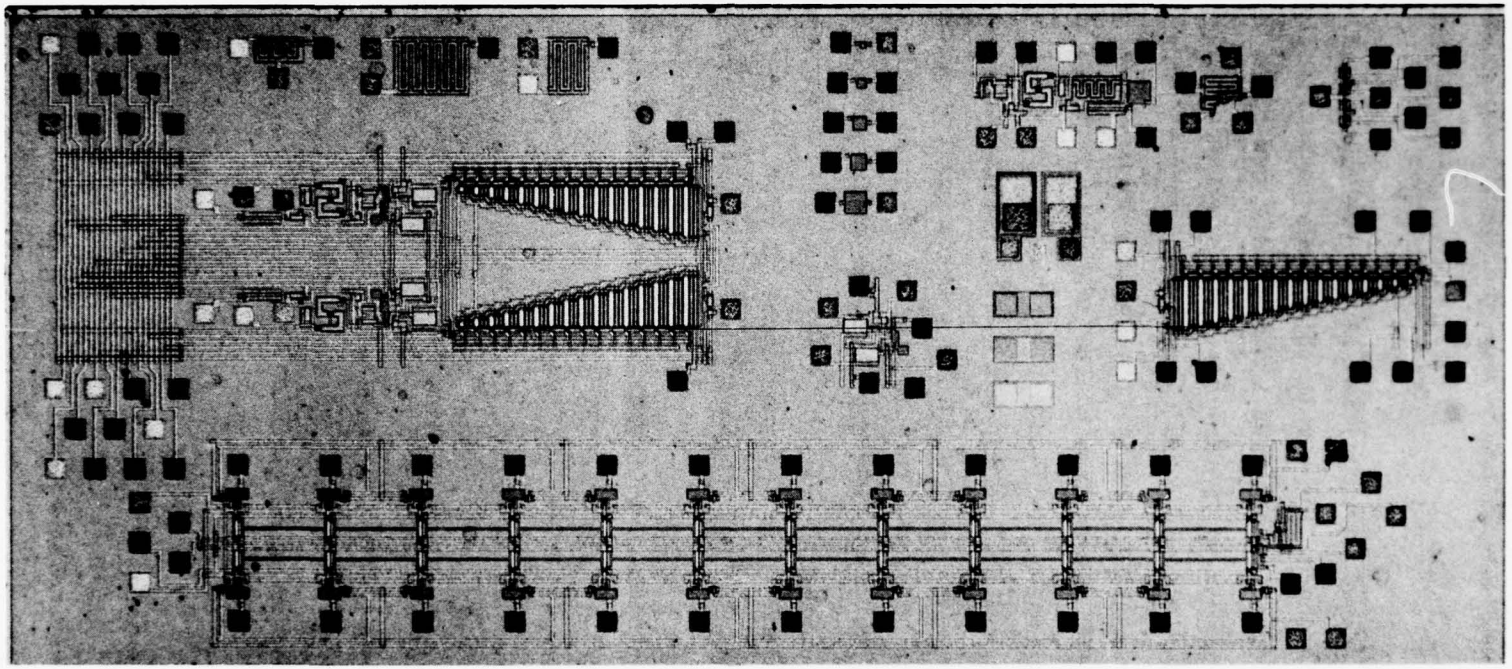


Figure 17 Test Chip Micrograph

and the output drives an additional source-follower stage, which was included to provide buffering of the highly capacitive loads associated with packaging and testing. In preliminary tests the circuit exhibited a nominal voltage gain of 50 and a bandwidth of about 1 MHz. This measured bandwidth is considerably smaller than predicted (4.2 MHz), an effect that was initially attributed to excess stray capacitance due to the addition of bond pads at the compensation nodes. Subsequent examination of the structure revealed that the depletion load devices (M1 and M4 in Figure 8 of the previous section) had been inadvertently coded with inverted W/L ratios. This resulted in lower load conductances and drain currents with a corresponding decrease in bandwidth and increase in gain and input referred noise. Revised SPICE simulations confirmed the gain bandwidth values and predicted an input referred noise density of 11 $nV/\sqrt{Hz}$ at room temperature. Preliminary noise measurements at room temperature indicated a Johnson noise level of about 10 to 12 $nV/\sqrt{Hz}$, in good agreement with SPICE simulations.

Additional SPICE runs were accomplished to simulate 77 K operation using device parameters that incorporated the theoretical temperature dependence of mobility and threshold voltage. These simulations predicted a voltage gain of 35, bandwidth of 4 MHz, input referred noise voltage of 4.4 $nV/\sqrt{Hz}$, and power dissipation of 8 mW at 77 K. (A number of cryogenic applications of surface channel, enhancement mode MOS transistors have been reported[2,18] which indicate good correspondence between predicted and measured temperature dependence of device parameters.) Thus, in spite of the layout errors, preamplifier performance at 77 K was expected to be close to original estimates, with the exception of power dissipation which is predicted to be twice the design goal.

Preliminary low temperature tests resulted in the somewhat startling observation that preamplifier noise performance did not improve at 77 K. Rather, the input referred noise voltage measured at 77 K was very nearly the same value

measured at 300 K, about 11 nV/$\sqrt{\text{Hz}}$. This result suggested the existence of noise mechanisms that had not been considered in the original analysis. Subsequent investigation led to the identification of the buried channel devices that comprise the feedback elements R_f and R_s as probable sources of the unpredicted noise.

Further tests were conducted on individual transistors, and Figure 18 illustrates the measured noise performance of a surface channel enhancement mode device and a buried channel device having identical W/L ratios and drain currents. Below 100 kHz the noise in the surface channel device is dominated by the well-known 1/f component due to surface states. This component exhibits a dependence on gate-source voltage that is between $V_{GS}^{\frac{1}{2}}$ and V_{GS}. The increased g_m at 77 K results in a lower V_{GS} to achieve the same drain current, and the 1/f component is also observed to decrease.

Buried channel devices exhibit low frequency noise due to generation-recombination centers (typically gold) that have a power density spectrum described by $(1 + \omega^2\tau^2)^{-1}$, where τ is related to trap emission times and is on the order of a few milliseconds at 300 K. At 77 K, however, τ is on the order of 10^{15} seconds, and, in the absence of other noise sources, only the Johnson-Nyquist component $[(8/3)\ (kT/g_m)]^{\frac{1}{2}}$ should be observed. From Figure 18 we note that the noise performance at 300 K is as predicted, with the high frequency noise floor very near the calculated Johnson-Nyquist value. At 77 K, however, the noise has clearly increased, indicating the presence of an unaccounted noise source.

In a paper on low frequency generation-recombination noise in junction FETs, Sah[19] compared the power spectra of various g-r sources and concluded that, although the component due to g-r centers in the gate depletion region was dominant at low frequencies, the component due to g-r mechanisms at donor sites would become appreciable at low temperatures. The solid curves in Figure 19

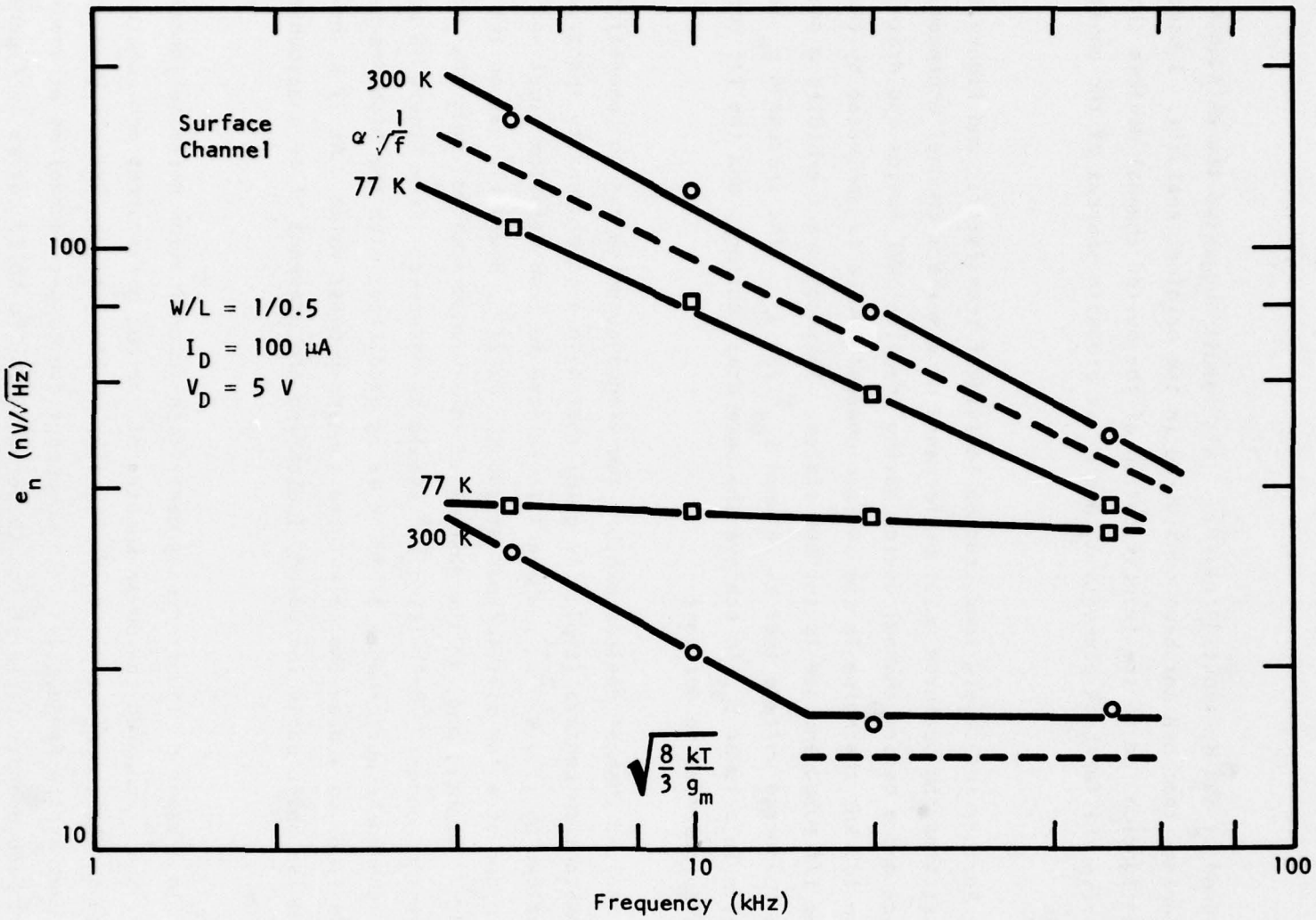


Figure 18 Comparison of Equivalent Gate Noise Voltages for Surface and Buried Channel MOSFETs at 300 K and 77 K

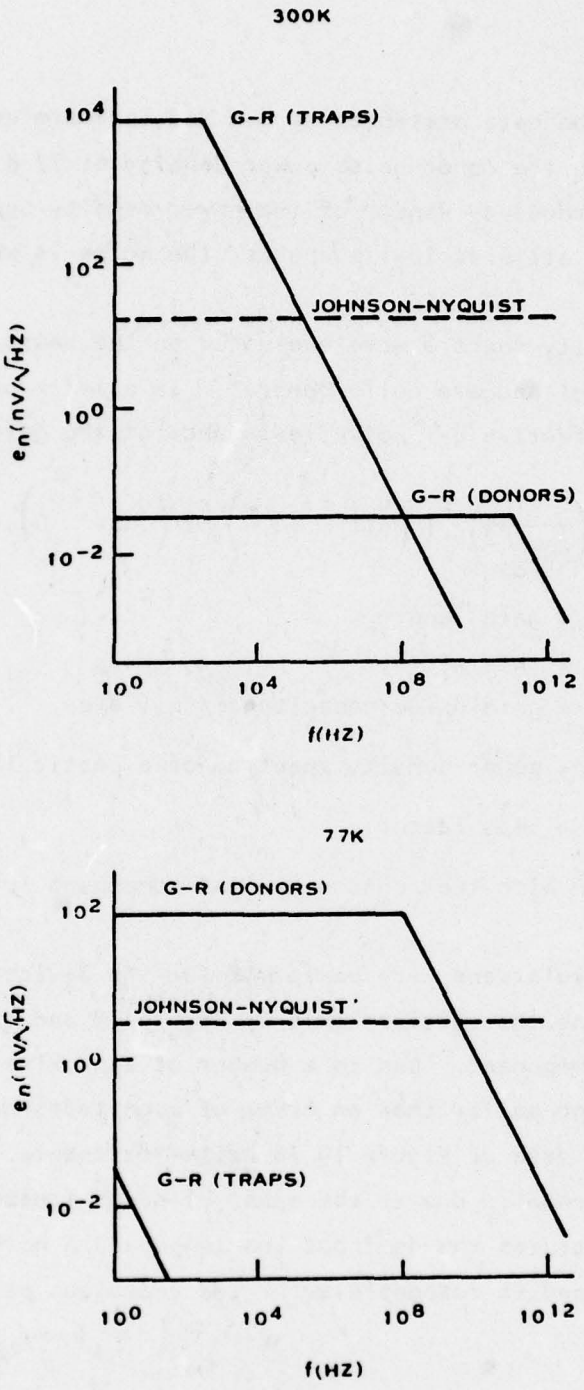


Figure 19 Theoretical Buried Channel Noise Performance

were evaluated from the data presented by Sah and indicate an increase of six orders of magnitude in the donor noise power density at 77 K over that at 300 K. (Note that the high frequency "knee" of the power density spectrum is at about 100 MHz at 77 K. For all practical purposes, the noise is white.)

These power density spectra were evaluated on the basis of g-r statistics in a conducting channel and are quite general. In a later publication, Yau and Sah[20] computed the effective g-r noise resistance at the gate with the result

$$R_{gn} = \frac{q^2}{3kT}\left(\frac{1}{LWC_{ox}^2}\right) F_1\left(N_{TT}, \tau_T, \omega\right) F_2\left(V_{GS}', V_D\right) ,$$

where L = gate length,

W = gate width,

C_{ox} = gate oxide capacitance/unit area,

$F_1\ (N_{TT}, \tau_T, \omega)$ = power density spectrum of a particular g-r center, and

$F_2\ (V_{GS}', V_D)$ = bias factor.

This allows comparison with the Johnson-Nyquist component for which $R_{gn} = 2/3(1/g_m)$.

The required calculations were performed for the device parameters shown in Figure 18 and determine the vertical axis in Figure 19 and the relative level of the Johnson-Nyquist component. Due to a number of approximations, the relative accuracy is probably no better than an order of magnitude; however, the agreement with the experimental data of Figure 19 is quite reasonable.* It was concluded that the g-r noise mechanism due to the onset of donor freeze-out in the buried channel devices consittutes the dominant low temperature noise source in the preamplifier circuit and is responsible for the anomalous performance observed.

---

* A subsequent literature search uncovered two papers describing an identical mechanism in junction FETs[5,21] that confirms the analysis presented here.

A processor chip redesign was proposed to eliminate the buried channel devices from the preamplifier circuit so as to achieve the desired performance goals. Details of the alternative approach are presented in a later section of this report.

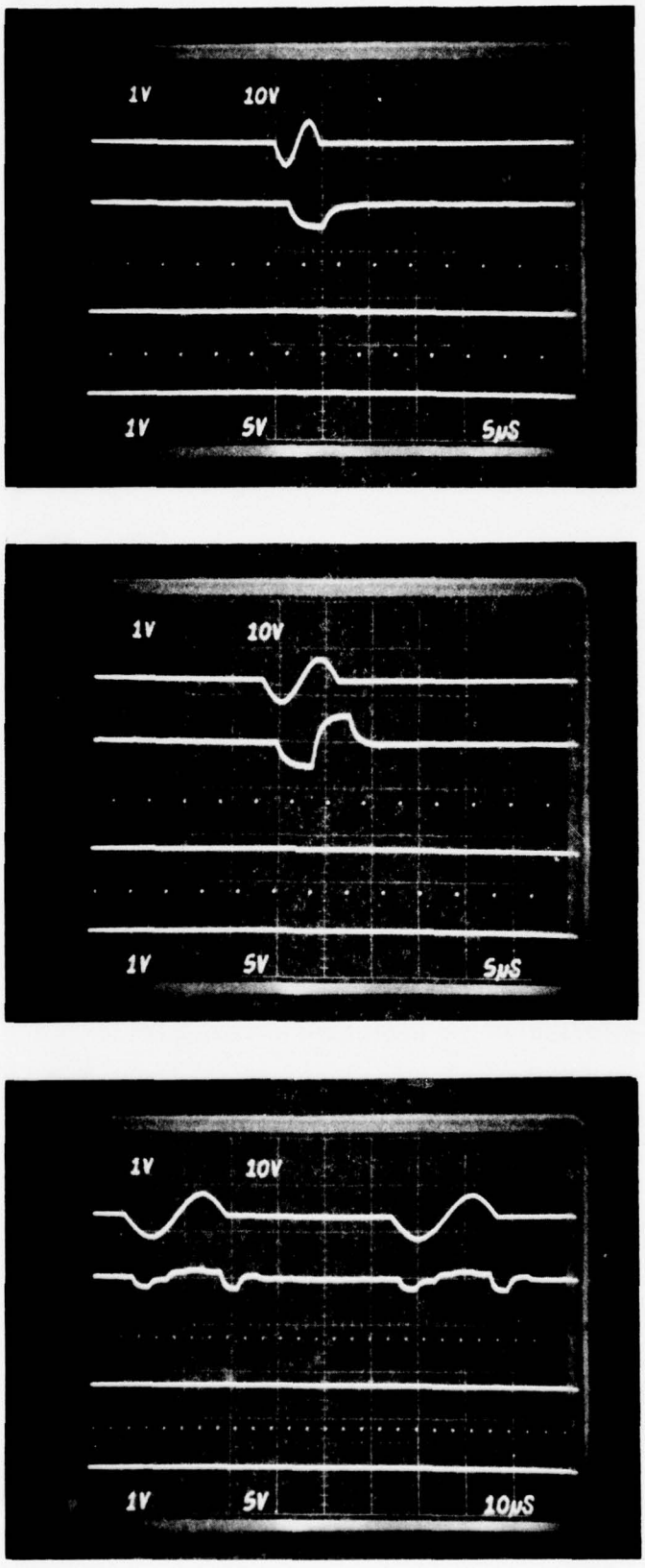
B. CDS Tests

The CDS test circuit is identical to the circuit used in the processor. It does not include an additional source-follower buffer stage, and the load capacitance is at least an order of magnitude larger than in the processor due to stray capacitances associated with packaging and testing. Operation of the CDS circuit at 300 K with 250 kHz clamp-and-sample rates is shown in the sequence of oscillographs in Figure 20. The test signal is a single cycle of a sine waveform, which is triggered in synchronism with the clock waveform. The clamp pulse is 50 ns in duration with a 10 V amplitude, while the sample pulse is 60 ns in duration with 4 V amplitude.

Voltage gain was measured with the sample switch closed and the reset switch closed periodically to establish the dc bias at the input. A voltage gain of 0.73 was observed. Output noise was measured and found to correspond closely to the theoretical value of 130 μV rms at 300 K.

C. TDI Tests

The TDI structure was tested at 300 K and determined to be operating very nearly as predicted with unity voltage gain. The oscillographs in Figure 21 show time-delay-and-integration of a rectangular pulse waveform. The resulting trapezoidal waveforms exhibit a modulo-three pattern due to the 3:1 interleave. The clock frequency in these photos is about 30 kHz (480 kHz input sample rate.)



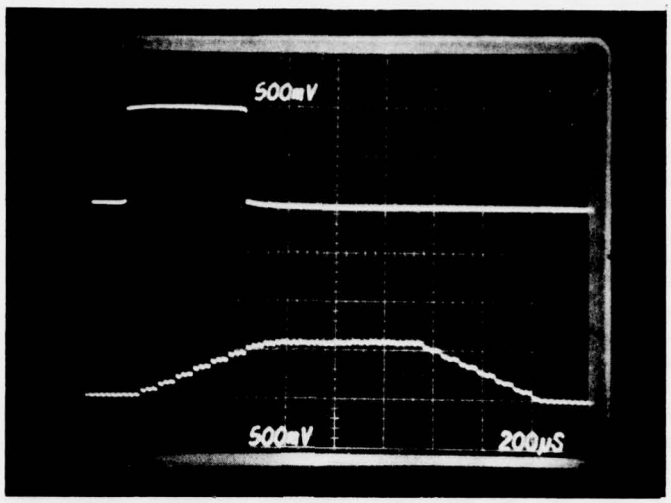
Input Waveform
1 V/div

Output Waveform
1 V/div

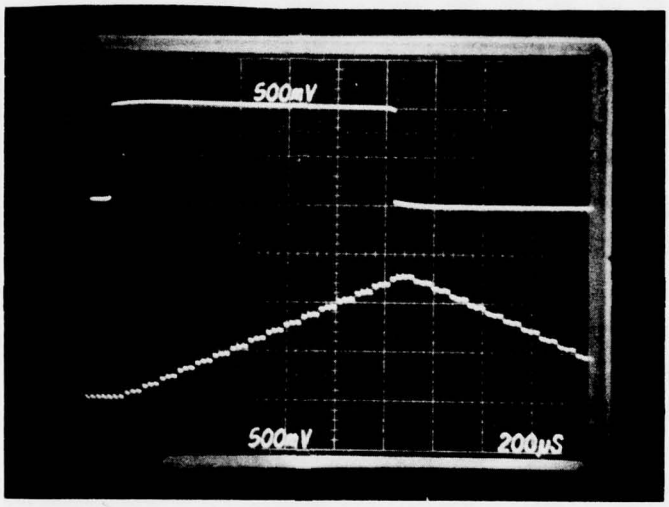
Clamp Pulse
10 V/div

Sample Pulse
5 V/div

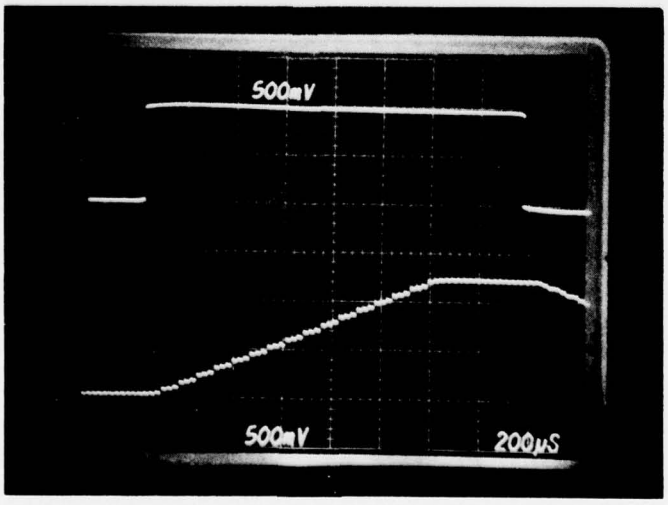
Figure 20 Operation of the CDS Test Circuit at a 250 kHz Rate



< 48 Cycles



48 Cycles



> 48 Cycles

Figure 21 TDI Test Photos

Further tests were conducted to evaluate the CTE in the demultiplexer. These tests involved clocking in a single signal charge packet, followed by a sufficient number of zero packets to ensure that no additional signal charge (other than "fat-zero") was entered into the TDI until the test signal was clocked through the entire structure. Further, the timing of the test signal was adjusted to allow the signal charge packet to propagate through a predetermined number of demultiplexer stages before being transferred into the summing register. The photographs in Figure 22 show the resulting TDI output and are labeled to indicate the number of stages traversed in the demultiplexer before parallel transfer. Evaluation of the CTE from these data yields a value of 0.94 for the floating diffusion transfers in the demultiplexer, as compared to the expected value of 0.99 at room temperature. Further investigation showed that the barrier lengths in the demultiplexer were 0.3 mil, rather than the desired 0.7 mil. Recalculation of the CTE expected for 0.3 mil gates results in a value that corresponds favorably with that observed.

An additional problem area is in evidence in the lower photograph for N = 16 in Figure 22. Poor CTE in the demultiplexer results in an error charge left in the floating diffusions following the parallel transfer into the summing register. This charge is clocked into the last demultiplexer cell when the next line is entered and results in an erroneous charge contribution that is subsequently transferred into the summing register. This problem can be remedied by adding an output diode to the demultiplexer which is held at a constant dc bias and acts as a drain for the extraneous charge.

The noise observed at the TDI output is dominated by reset noise on the input and output nodes and is predicted to be approximately 225 μV rms at 300 K. The measured output noise level (on the basis of a single spot noise measurement at 50 kHz) is 210 μV rms, which corresponds favorably with the above.

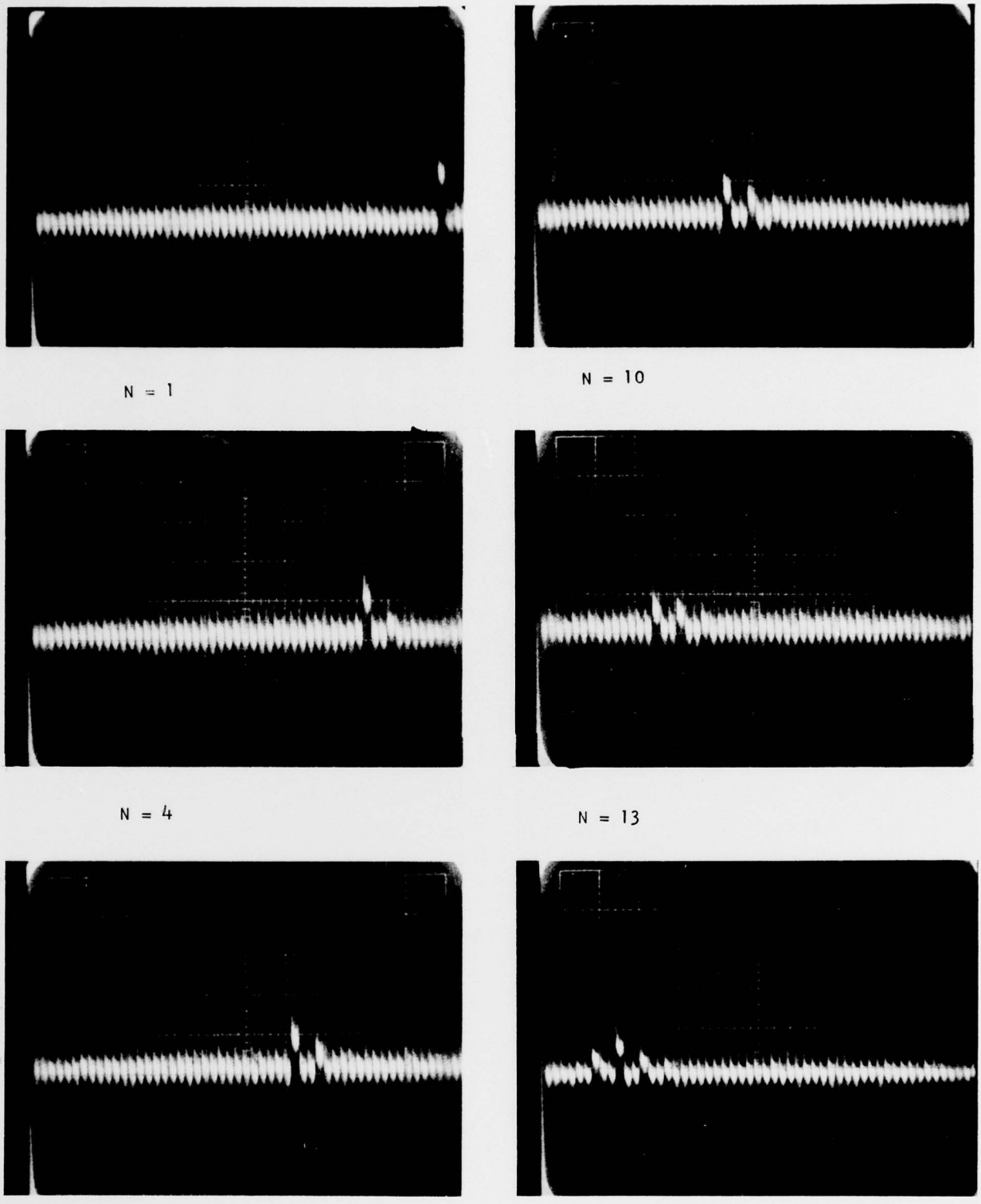
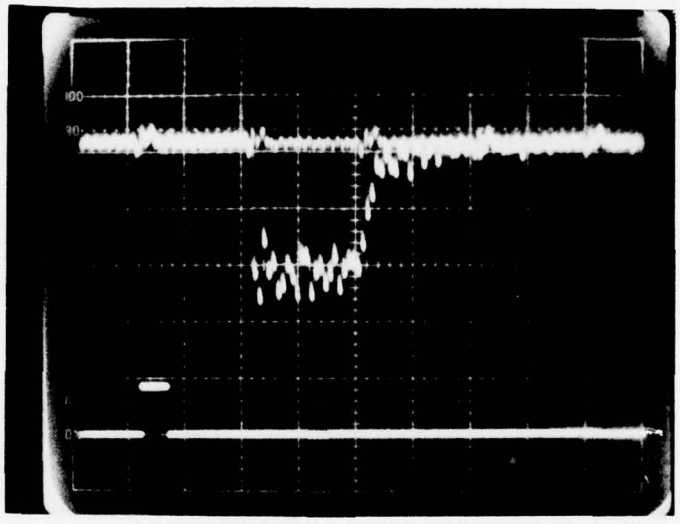


Figure 22 TDI Output Due to a Single Charge Packet Which Has Propagated Through the Indicated Number of DEMUX Transfer Stages. (Vertical: 50 mV/div; horizontal: 100 μs/div.)

D. Multiplexer Tests

Preliminary tests performed on the output multiplexer test structure indicated a much lower CTE than expected. A subsequent recheck of the geometry revealed that, as in the TDI demultiplexer, the barrier lengths in the transfer cell adjacent to the floating diffusion were shorter than intended. In addition, the fixed pattern noise component was observed to be more than an order of magnitude larger than expected. Figure 23 shows the response of a typical device to a rectangular input pulse applied at the dc restore port. All ac-coupled inputs were grounded. Note that the fixed pattern noise observed on the output waveform is approximately 200 mV peak-to-peak. The voltage gain through the multiplexer was measured to be about 0.2, a factor of three smaller than expected, resulting in an input referred fixed pattern noise amplitude of nearly 1 V.

Further analysis indicates that the cause of the large fixed pattern noise component is potential barriers that exist at the edge of a fully implanted second-level polysilicon gate. The presence of these barriers was confirmed by tests on dual-gate transistors that were fabricated on a previous IC using the same polysilicon gate process. The barriers are believed to be caused by undercutting of the first-level gates, which results in an extension of the second-level gate beyond the edge of the ion-implanted region. The amount of undercutting is not controlled and can be expected to vary significantly among devices on any particular chip. This affects the height and width of the resulting barrier and can result in appreciable differences in the amount of charge transferred into and out of the storage well in the multiplexer input circuit. In addition to the fixed pattern noise, it is believed that the presence of these barriers is responsible for the reduced gain and the abnormally high voltage that must be applied to the dc restore terminal to cut off charge injection into the receiving well.



MUX OUT

200 mV/div

Input signal at
dc restore
5 V/div

Horiz. 10 μs/div

Figure 23 Multiplexer Operation with Test Signal Introduced at the dc Restore Terminal

The topology of the multiplexer input circuit is sketched in Figure 24(a), where the location of the barriers is indicated by the small arrows. Figures 24(b) through 24(d) illustrated the formation of the signal charge packet and its subsequent transfer into the multiplexer channel. Note that the barriers are directly involved in both charge packet formation and transfer.

Formation of the signal charge packet is illustrated further in Figure 25, which compares ideal input circuit operation with that including the potential barriers. Figure 25(a) corresponds to near "full-well" conditions, where the charge packet equals the maximum charge capacity of the multiplexer structure. Note that the fringing fields between the input gate (IPG--connected to the dc restore switch is the previous figure) and the input well lower the effective height of the barrier . In Figure 25(b) the voltage on IPG has been adjusted to achieve a "half-well" condition in the ideal case. However, due to a reduction in fringing fields the effective barrier height increases, resulting in substantially more than "half-well" charge. Finally, in Figure 25(c), the voltage on IPG is sufficient to allow all signal charge to "spill" back into the input diode (IDD), resulting in a zero charge packet. The presence of the barrier results in the formation of a substantial charge packet for this case, and the voltage on IPG must be further increased to lower the barrier to the cutoff point, as observed in the tests.

This phenomenon is summarized in Figure 25(d), which shows the relation between the charge packet Q_s and the difference $V_{IPG}-V_{WELL}$. In the usual operating regime the dependence is linear and has slope equal to the capacitance of the well electrode, C_{WELL}. The effect of the barrier is to lower the slope, resulting in a lower effective well capacitance and, therefore, lower gain through the multiplexer.

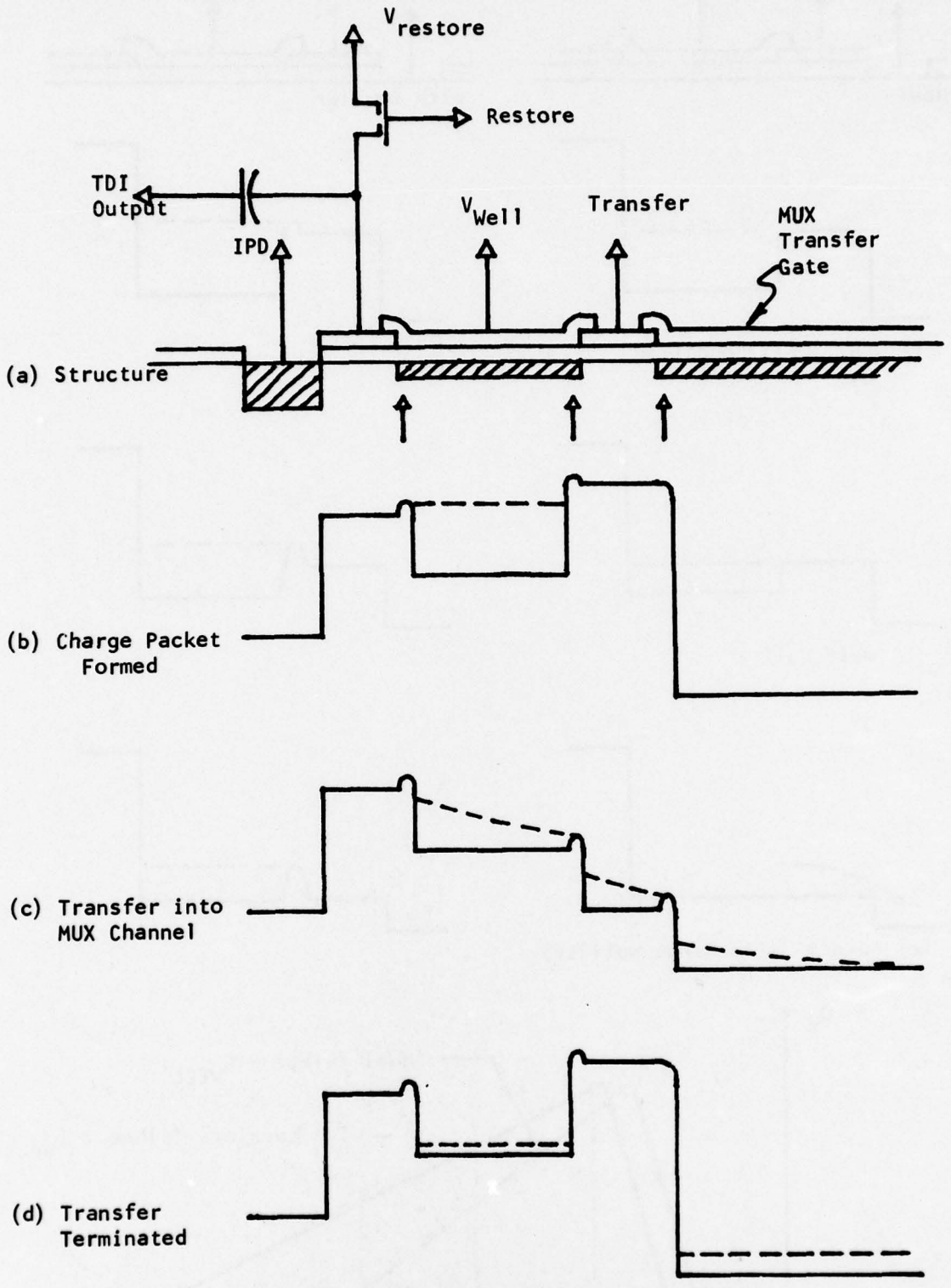


Figure 24 Multiplexer Input Circuit

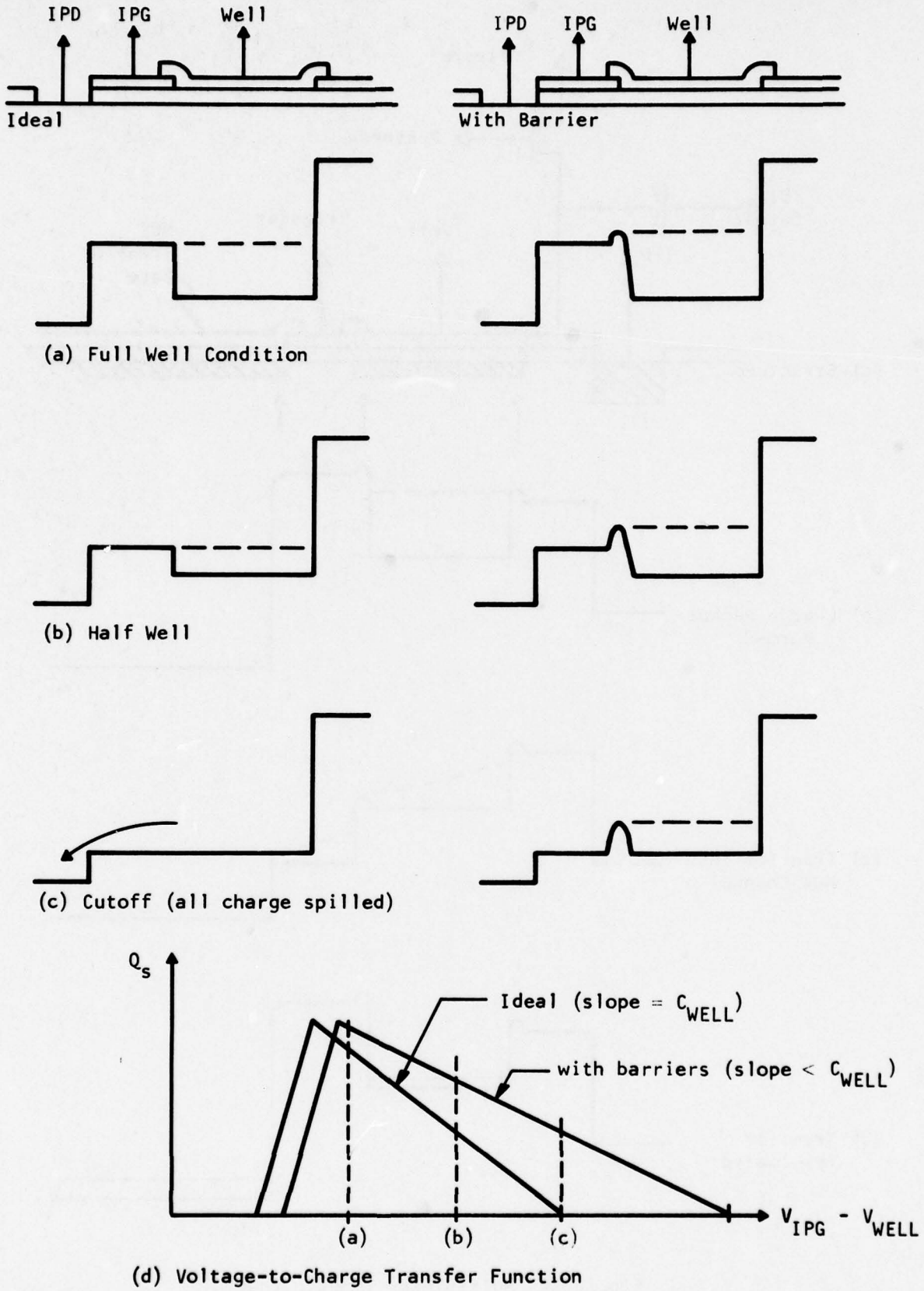


Figure 25 Effect of Potential Barriers in the Multiplexer Input Circuit

The presence of the barriers was troublesome in other chip designs, and a process modification was identified (subsequent to processing the silicon processor chips) that eliminates the problem.

Figure 26 illustrates the response of the multiplexer to a triangular test waveform applied at the dc restore port. The fixed pattern noise is approximately 500 mV peak-to-peak, half due to barrier-induced level variations (as in Figure 23) and half due to a slope on each 24-sample output burst caused by the low CTE.

E. Processor Bar Tests

Although serious problems exist in the preamplifier and multiplexer designs, testing of a complete processor bar was accomplished to confirm proper interconnection of the components. Preliminary tests of the processor bar were accomplished by testing individual components, using operating parameters determined during evaluation of the test structures, then optimizing those parameters for overall processor operation.

The multiplexer was first adjusted for proper operation by applying a test waveform at the $V_{restore}$ terminal and a control pulse at the restore terminal such that the dc-restore circuit operated as a sample-and-hold driving the multiplexer input gate. Next, the TDI circuit was adjusted for proper operation by applying a test signal at the V_{clamp} terminal of the CDS circuit and monitoring the TDI output with a microprobe at the output source-follower. The CDS circuit thus double-sampled the test waveform, which was then applied to the demultiplexer input gate. A typical output waveform is shown in Figure 27, illustrating proper operation of the CDS and TDI circuitry. The $V_{restore}$ terminal was then connected directly to a dc power supply, and the restore pulse was furnished once every 200 samples to perform the dc-restore function at the multiplexer input. After a minor timing problem was solved, proper operation of the combined CDS, TDI, and MUX circuitry was observed, as illustrated in the sequence of photos in Figure 28.

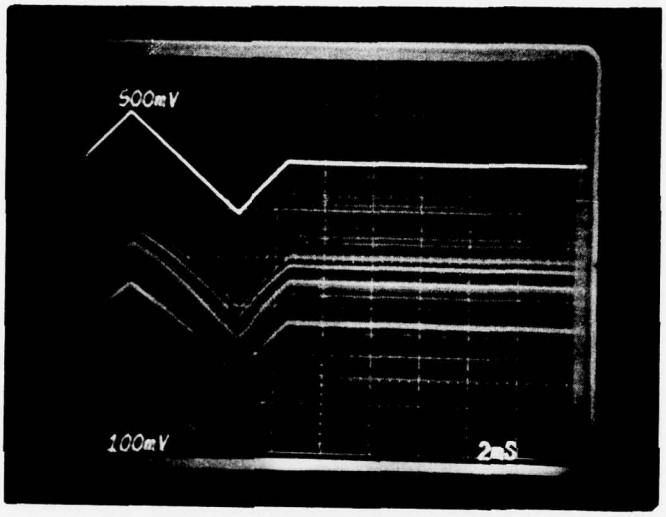
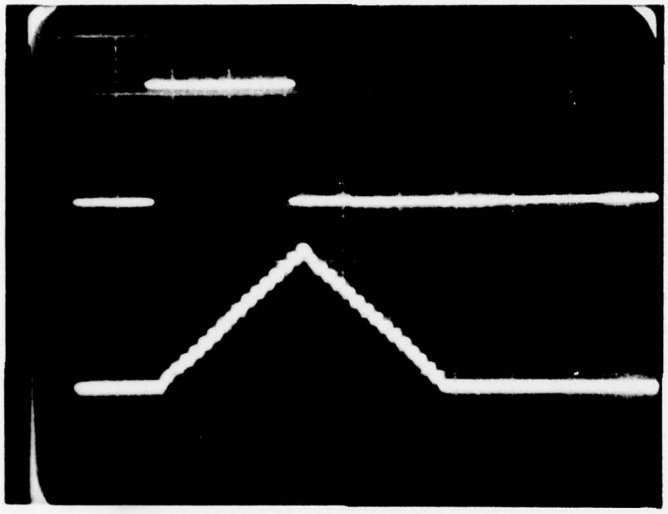


Figure 26 Multiplexer Response to a Triangular Test Waveform Applied at the dc-Restore Port



Input Waveform at V_{clamp} Terminal
500 mV/div

Output Waveform With Microprobe at Source-Follower
500 mV/div

Horizontal 2 ms/div

Figure 27 Operation of CDS and TDI Circuits on the Processor Chip

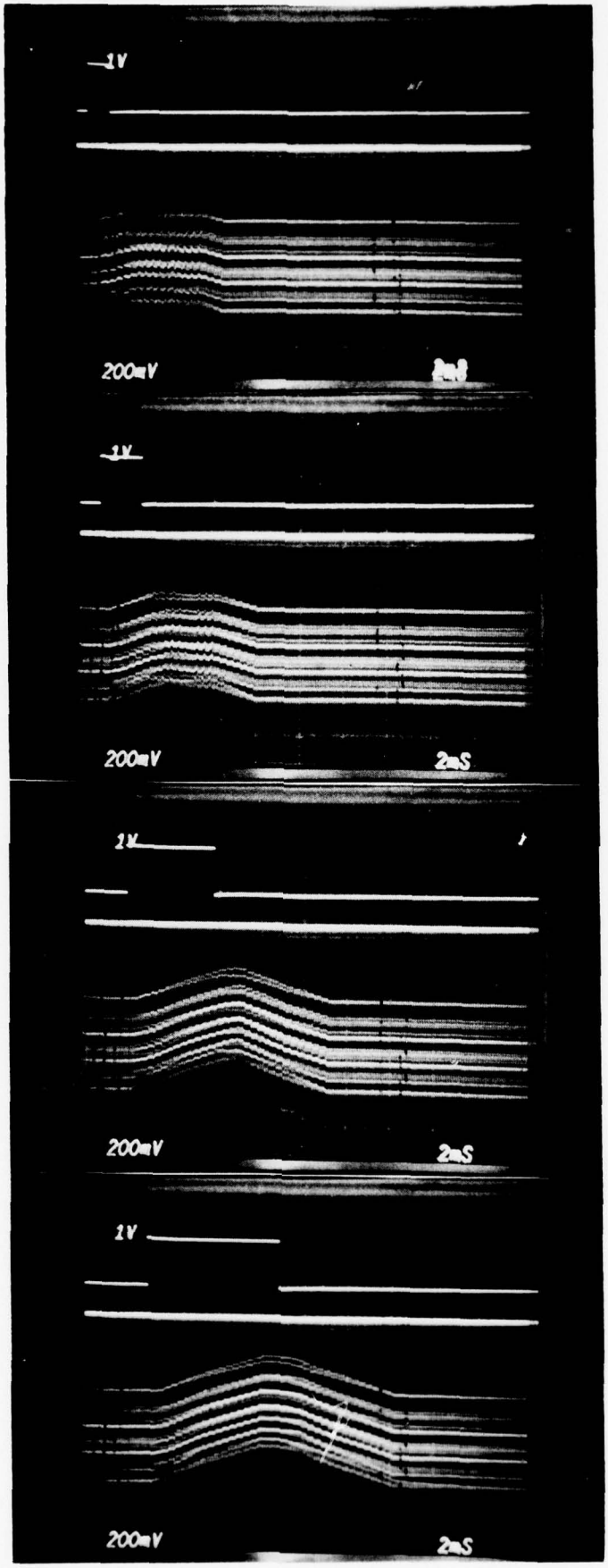


Figure 28 Operation of the CDS, TDI, and MUX Circuits

Operation of a single channel through a preamplifier input has been observed, but the large fixed pattern noise at the multiplexer makes it very difficult to discern a single operating channel.

Due to the serious problem observed in the preamplifier and multiplexer and, to a lesser extent, in the TDI, it was apparent that a processor redesign was required to meet the performance goals discussed in Section II of this report. The problem areas discussed in this section were believed to be well understood, and alternatives were identified and analyzed. Details related to the redesign of each circuit are described in Section V.

SECTION V
PROCESSOR REDESIGN

The main problem areas discussed in the previous section that were addressed in the redesign are:

(1) Replacement of buried channel feedback devices in the preamplifier
(2) Extension of barrier lengths in TDI demultiplexer
(3) Addition of output diode drain circuit to TDI demultiplexer
(4) Extension of barrier lengths in multiplexer
(5) Elimination of potential barriers in the multiplexer input circuits.

It was anticipated that the barrier problem would be corrected with the new process modification mentioned in Section IV. Plans also included adding a serial fat zero input circuit to the multiplexer structure to improve CTE.

Details of the redesign of each circuit are presented in this section. In each case the redesign was accomplished with minimal modification to the existing structure, and no modifications in the interconnections were required.

A. Preamplifier Redesign

The low noise preamplifier was completely redesigned to eliminate the buried channel feedback devices and to exploit improved device parameters at 77 K. A schematic diagram of the new circuit is shown in Figure 29. The feedback devices have been realized with polysilicon thin film resistors. The first polysilicon level exhibits a sheet resistance of approximately 65 Ω/square and is doped by a phosphorus implant with a resulting donor density in excess of $10^{20}/cm^3$. At this density barrier effects at grain boundaries are negligible, and the properties of the thin film should approximate those of single crystalline material with a lower mobility caused by the additional scattering due to defects.[22] In addition, the large donor density should result in reduced temperature dependence of resistivity due to impurity scattering.[23]

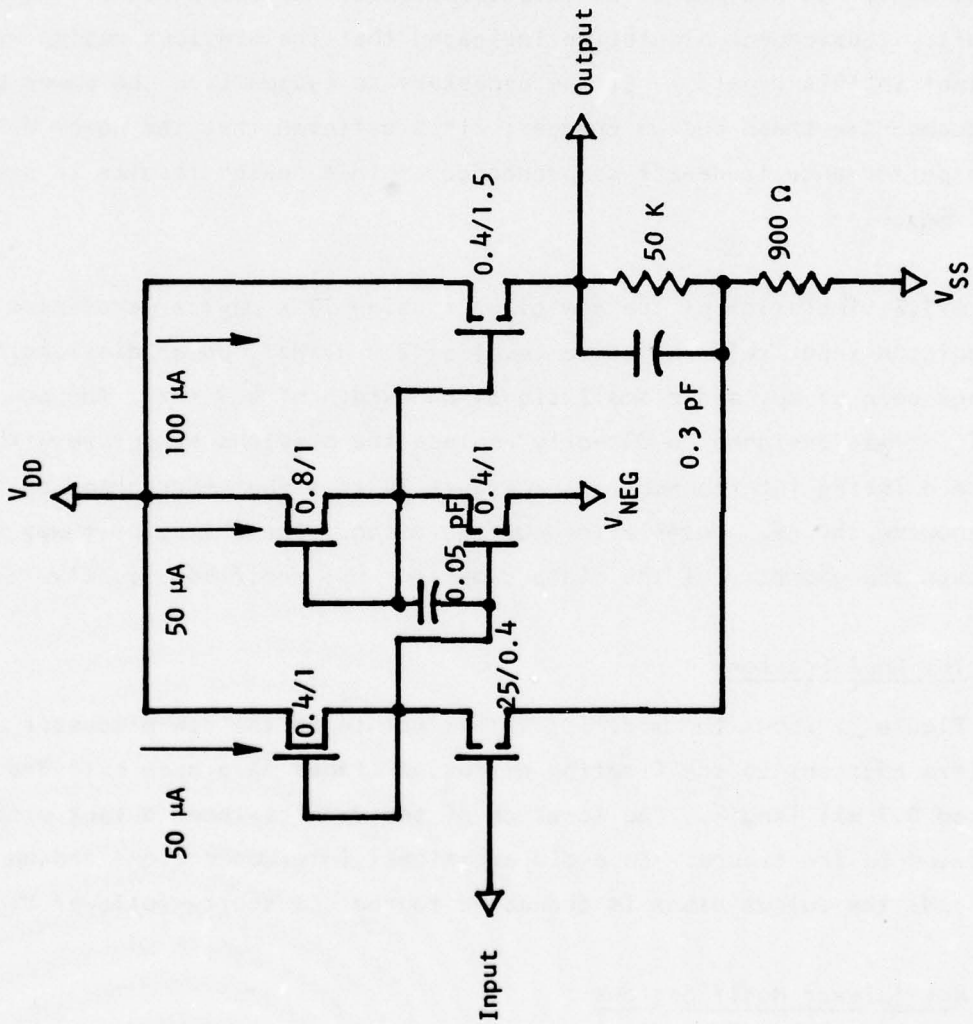


Figure 29 Schematic Diagram of the Redesigned Preamp

The value of the feedback resistors has been reduced to minimize their contribution to Johnson noise. The source-follower stage is now used as an output buffer to provide a low output impedance for operation of the CDS circuit. (Subsequent simulation indicated that the previous design was marginal in this regard.) It was necessary to reapportion the power budget to accommodate these design changes; it is believed that the power dissipation - noise performance trade-off comprehended in this design results in nearly optimal performance.

SPICE simulation of the new cirucit using 77 K device parameters indicates a predicted input referred noise level of 2.9 $nV/Hz^{\frac{1}{2}}$, power dissipation of 4.1 mW, voltage gain of 40, and a small signal bandwidth of 4.3 MHz. The new preamplifier was designed to directly replace the previous structure with no changes to the existing interconnections. Figure 30 is a photomicrograph of the completed bar showing the new preamplifier configuration. The CDS circuit was not changed, although the geometry of the clamp capacitor was modified slightly.

B. TDI Modification

Figure 31 shows the modified TDI structure on the new processor chip. The barriers adjacent to the floating diffusion stages have been extended to the desired 0.7 mil length. The location of the demultiplexer output diode is indicated in the figure. To avoid additional interconnections and an extra bond pad, the output diode is connected to the TDI source-follower V_{DD} line.

C. Multiplexer Modifications

Figure 32 shows the modified multiplexer structure. Comparison with Figure 15 in Section III shows that the second-level gates have been extended to achieve the desired barrier length.

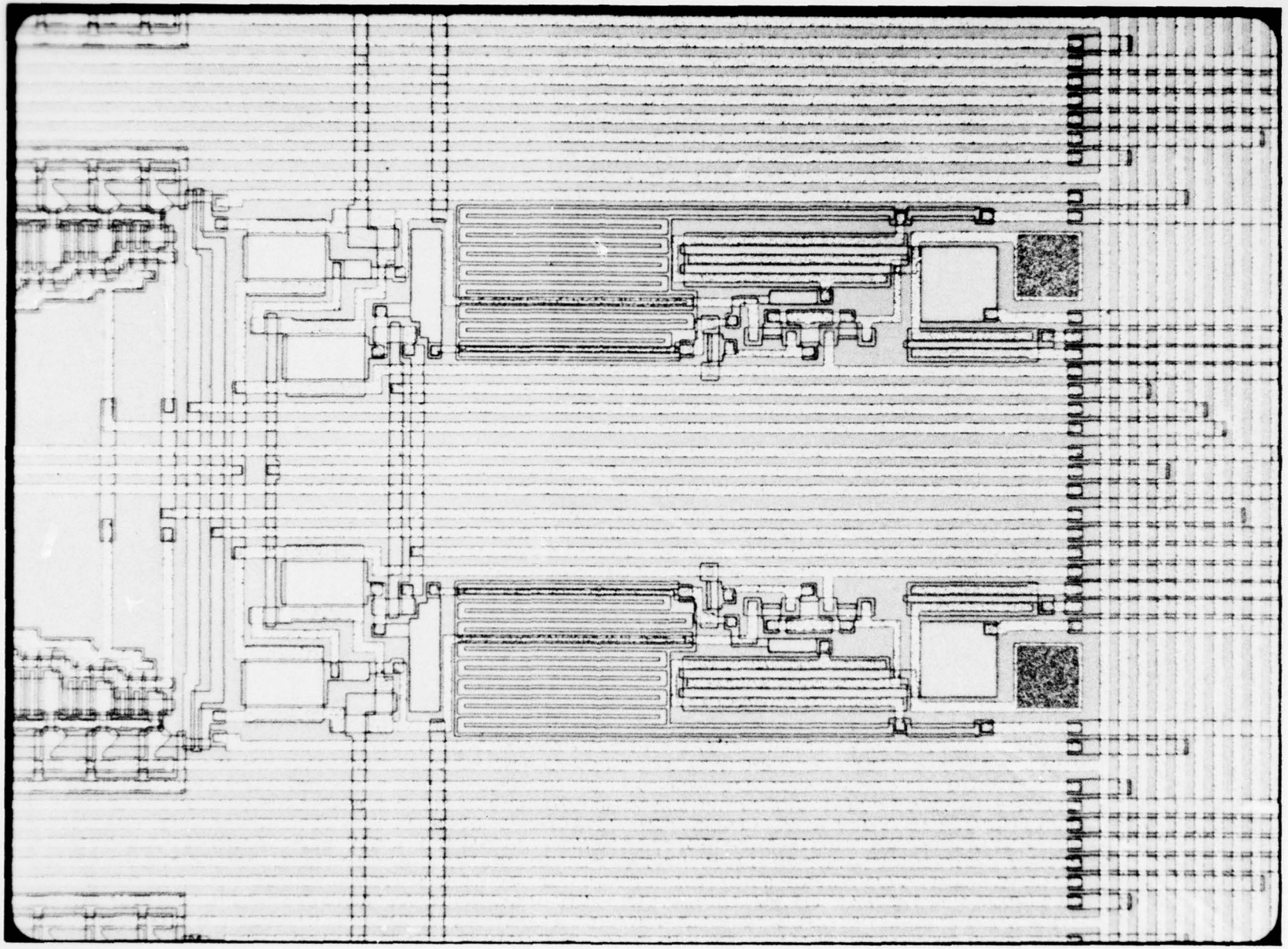


Figure 30 Photomicrograph Showing the Structure of the Redesigned Preamplifier

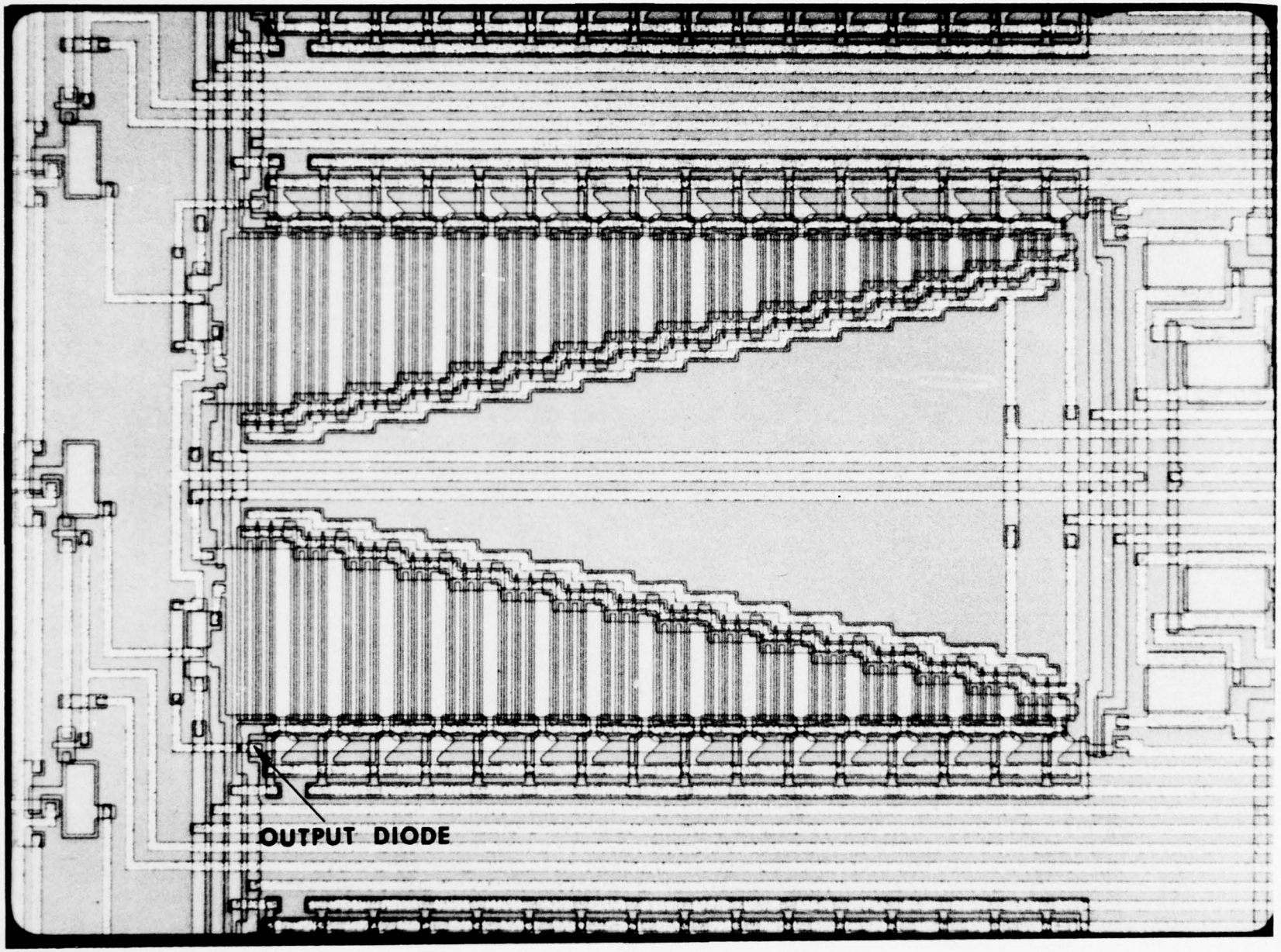


Figure 31 Photomicrograph of the Redesigned TDI Structure Showing the Location of the Output Diode

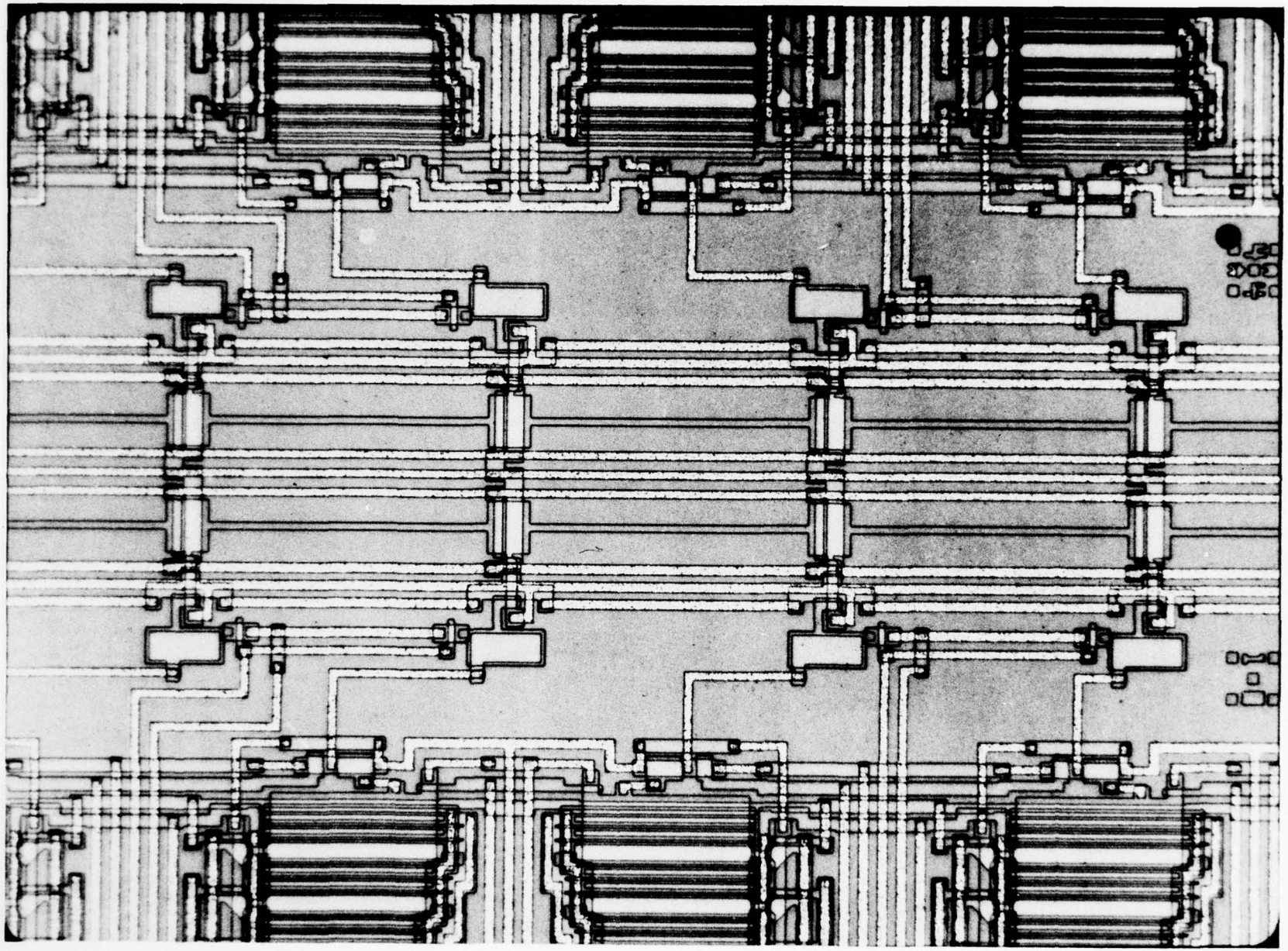


Figure 32 Photomicrograph Showing the Structure of the Multiplexer

Figure 33 is a photomicrograph of the entire processor bar. The serial fat zero circuit added to the multiplexer can be seen in the upper-center portion of the photo. Figure 34 shows the test bar which was reconfigured by deleting the dual-channel processor test structure and rearranging the individual component test structures to allow their interconnection to form a complete processor channel. A separate preamplifier test circuit is included that allows bonding of input transistors having W/L ratios of 100, 150, and 200. In addition, this test structure includes separate bond pads for each V_{DD} connection, thus allowing external measurement of the current in each stage.

The results of the tests performed on the new devices are presented in Section VI.

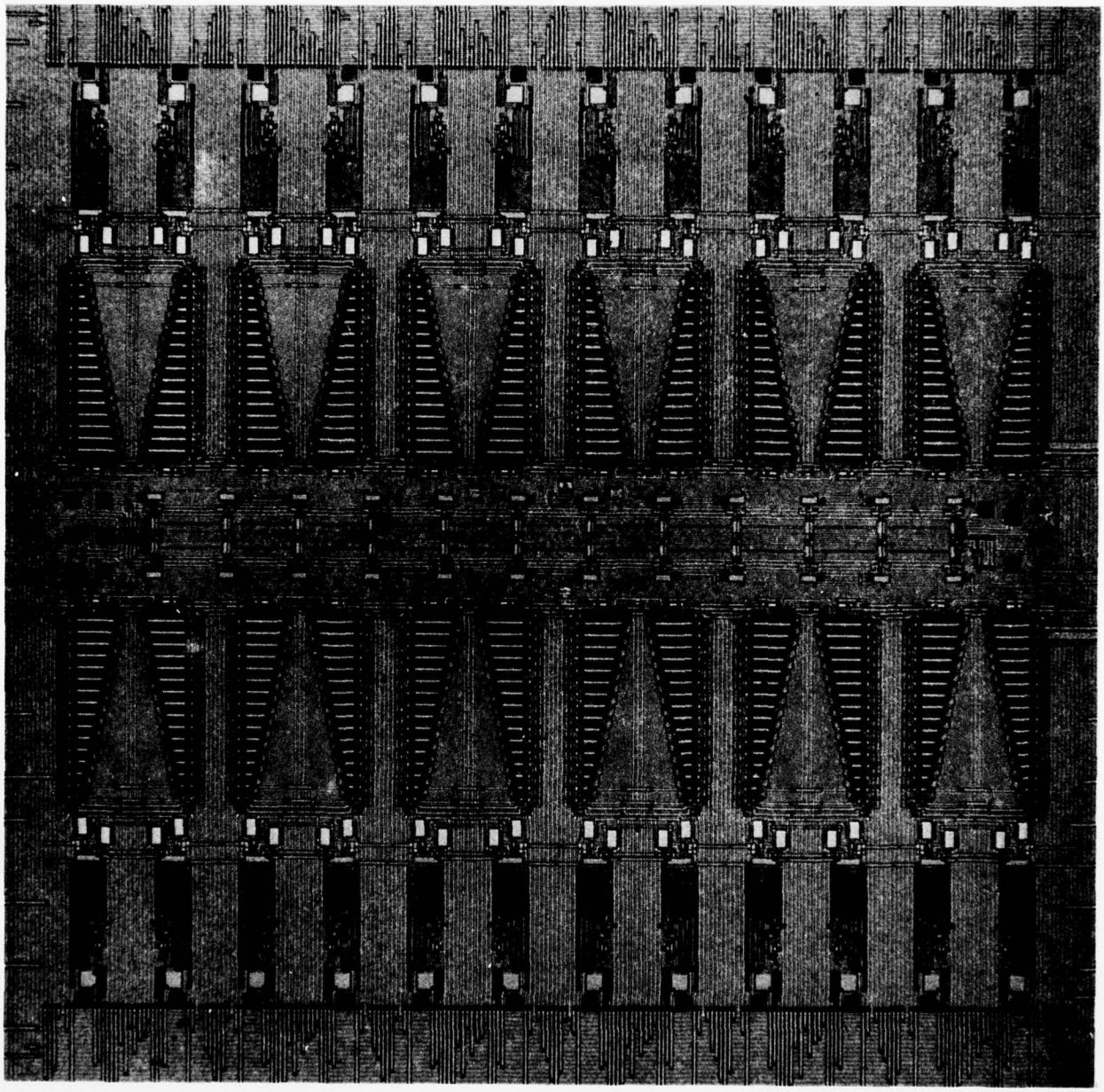


Figure 33 Photomicrograph of the Completed Processor Chip

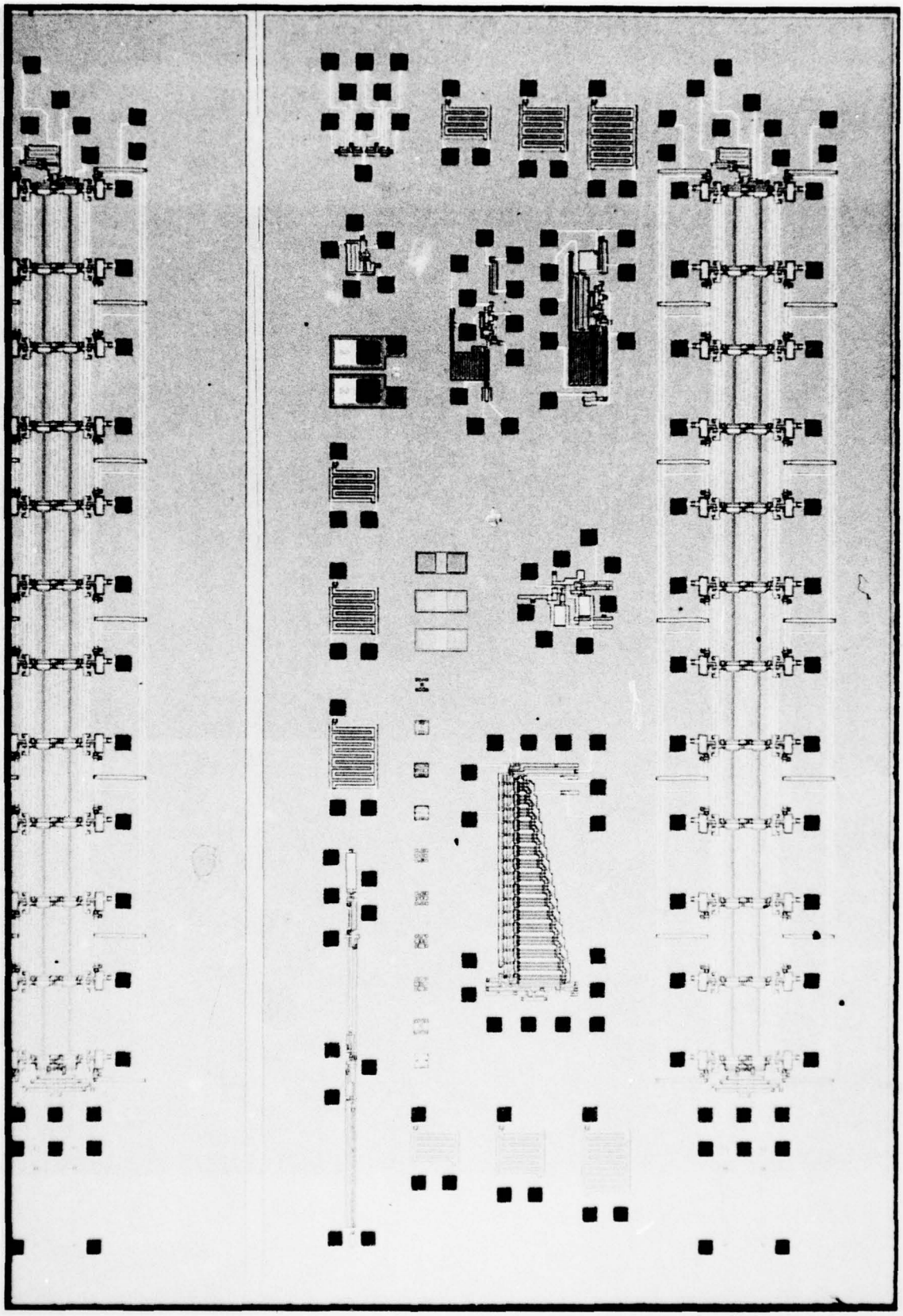


Figure 34 Photomicrograph of the New Test Bar

SECTION VI

EVALUATION OF REDESIGNED COMPONENTS

A. Preamplifier Evaluation

Room temperature tests indicate excellent agreement with 300 K SPICE simulations. Preamplifier gain is approximately 30 with a 1.5 MHz bandwidth and an input referred noise level of about 10 nV $Hz^{\frac{1}{2}}$. The low voltage gain is due to the additional output buffer stage used in the test circuit to drive the high capacitance load associated with packaging and testing. Circuit performance at 77 K is considerably below SPICE prediction, however. Although the voltage gain is maintained (indicating good tracking of the polysilicon feedback resistors), a -3 dB bandwidth of 2 MHz and input referred noise level of 5nV/$Hz^{\frac{1}{2}}$ have been measured, compared with predicted values of 4.2 MHz and 2.9 nV//$Hz^{\frac{1}{2}}$, respectively. Voltage gain and input referred noise level are plotted as functions of frequency in Figure 35.

Further tests were conducted using the additional preamp test structure which included separate V_{DD} bond pads for independent measurement of stage bias currents. These tests indicated a severe decrease in the dc bias current in the two inverter stages at 77 K. Measured values were about 5 μA in each stage, as compared with design values of 50 μA. An order of magnitude decrease in the bias current in the first stage results in an increase of about 1.8 in the Johnson noise level of the input transistor and accounts for the degraded noise performance. Subsequent tests indicated that the conductance of the depletion load devices was a factor of 3 to 4 lower than expected (nearly equal to room temperature values), which results in the lower bandwidth observed.

Additional tests were performed on individual depletion mode test transistors and revealed the existence of freeze-out effects similar to those observed in the buried channel devices. Enhancement mode transistors do not exhibit freeze-out

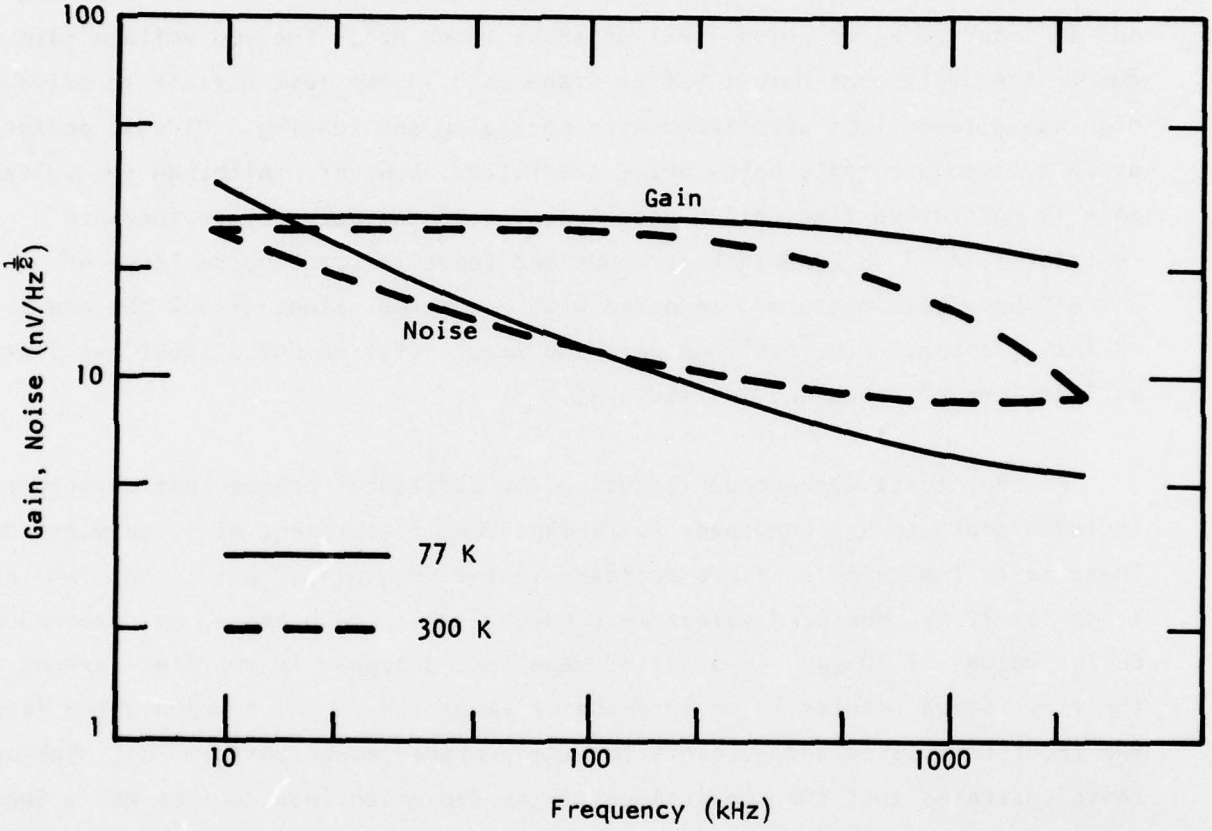


Figure 35 Voltage Gain and Input Referred Noise in the Preamplifier at 300 K and 77 K

effects because of the strong depletion fields that exist near the surface. Any mobile holes in this region are swept into the bulk, therefore maintaining full ionization of the acceptor sites in the region of the conducting channel.

The effect of the depletion implant is to introduce a sheet of donor atoms near the semiconductor-oxide interface. Since the depletion fields act to confine mobile electrons near the interface, the implanted donors are subject to freeze-out effects. Figure 36 is a plot of $(I_D)^{\frac{1}{2}}$ vs gate-source voltage measured at 300 K and 77 K for a depletion transistor having a W/L ratio similar to that of the load devices in the preamp. Also shown in the figure is the dependence predicted by SPICE for 77 K operation. (SPICE predictions at 300 K are in excellent agreement with the measured data and are not presented separately.) Ideally, the dependence should be linear, having a slope proportional to the effective surface mobility μ_s and a y-intercept equal to the threshold voltage of approximately -3.5 V.

The 77 K data, however, are clearly nonideal and are characterized by a knee in the dependence that occurs at slightly positive gate-source voltages. Although the threshold shift is larger than predicted, this is not the dominant discrepancy. At low drain currents the effective surface mobility is approximately equal to that observed at room temperature, whereas SPICE predicts an increase in μ_s by a factor of 3 at 77 K due to its $T^{-3/2}$ temperature dependence. Since $V_{GS} = 0$ for the depletion loads in the preamp, the measured drain current in this test is a factor of 10 lower than predicted by SPICE. Back-gate bias effects are observed to push the knee toward lower values of I_D.

A detailed analysis of freeze-out effects in depletion mode transistors has been performed and appears in Appendix B. A brief explanation of the effect is summarized in the following:

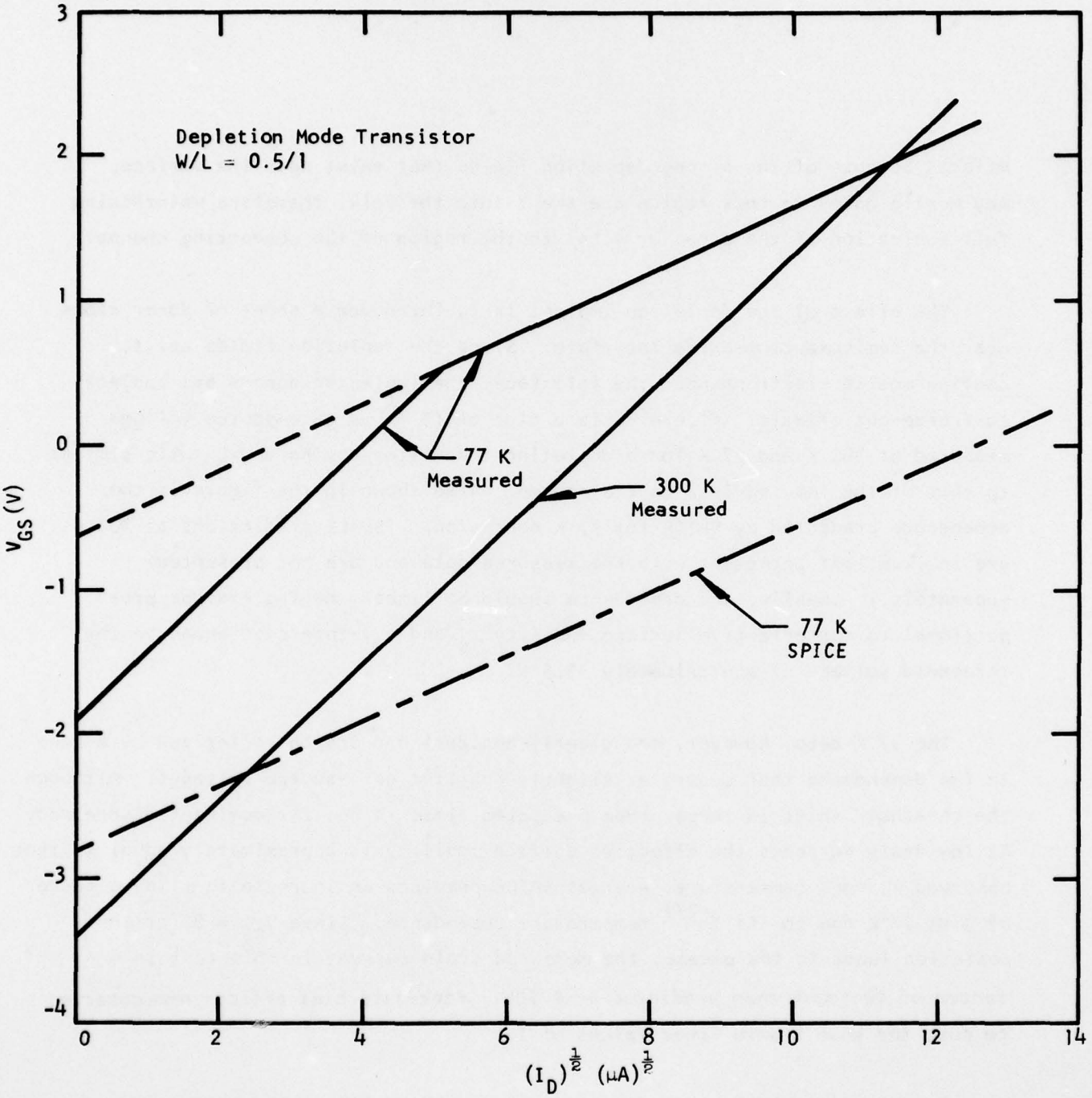


Figure 36 Measured and Predicted Performance of a Depletion Mode Transistor Showing the Effects of Donor Freezeout

- At the onset of conduction ($V_{GS} \sim V_T$) the channel is depleted of electrons due to source and drain depletion regions, and all implanted donors are ionized. Thus, the threshold voltage is, to first order, unaffected by low temperature operation (except for an expected shift due to the temperature dependence of the bulk Fermi level).

- As additional charge is added to the gate electrode, an image charge is induced at the semiconductor-oxide interface. This charge is furnished by the source diffusion, and in enhancement devices it consists solely of mobile electrons, resulting in drain current. In the depletion device, however, a portion of this charge becomes bound to previously ionized donor atoms. The rest of the charge contributes to the drain current. The exact ratio between bound and mobile charge depends on the relative positions of the donor level and the electron quasi-Fermi level in the semiconductor energy gap. The overall result, however, is a gate voltage dependence of the threshold voltage which can be modelled as a lower effective surface mobility.

- At some larger value of the gate voltage, the implant in the vicinity of the surface charge sheet will be completely frozen out, and further increases in gate charge will result in an equal increase in mobile surface charge and, therefore, in the drain current. All further increases in gate voltage result in increases in drain current consistent with the expected value of the mobility; thus, the g_m of the device will increase to its expected value. Extrapolation of this portion of the $(I_D)^{\frac{1}{2}}$ vs V_{GS} curve results in a second "threshold voltage" which is indicative of the extent to which the depletion implant is frozen out. The calculations in Appendix B show that nearly 80% of the charge in the depletion implant is frozen out at high gate-source voltages.

This mechanism imposes a severe restriction on the applicability of conventional analog MOS circuits to low temperature operation. The effect was completely unexpected (although, in retrospect, the earlier measurements on buried channel devices were indicative), and, to our knowledge, this is the first time such a mechanism has been observed in MOS devices.

B. CDS Tests

Although the CDS circuit was not redesigned, it was tested again during this evaluation to more carefully document its performance. The CDS circuit was tested at 100 kHz clock rate to minimize the effects of reduced bandwidth in the second source-follower stage due to heavy capacitive loading by the test equipment. Figure 37 illustrates the noise performance measured at room temperature at the CDS output node. The lower curve was obtained by closing the clamp and sample switches and corresponds to the quadrature sum of the 1/f and Johnson noise components of the source-follower stages. The upper curves represent the theoretical and measured output noise levels in normal operation. The difference between theoretical and measured levels is thought to be partially due to aliasing of the Johnson noise generated in the clamp buffer stage. This stage has a predicted bandwidth of approximately 10 MHz at room temperature, resulting in an aliased noise component of approximately 400 $nV/\sqrt{Hz}$ in the Nyquist interval. This value is within experimental limits of the excess noise component observed. The voltage gain of the CDS circuit was approximately 0.8.

Proper operation of the circuit was observed at 77 K, and spot noise measurements confirm the expected noise performance. Since the depletion load devices are externally biased, the freeze-out effect does not compromise circuit performance.

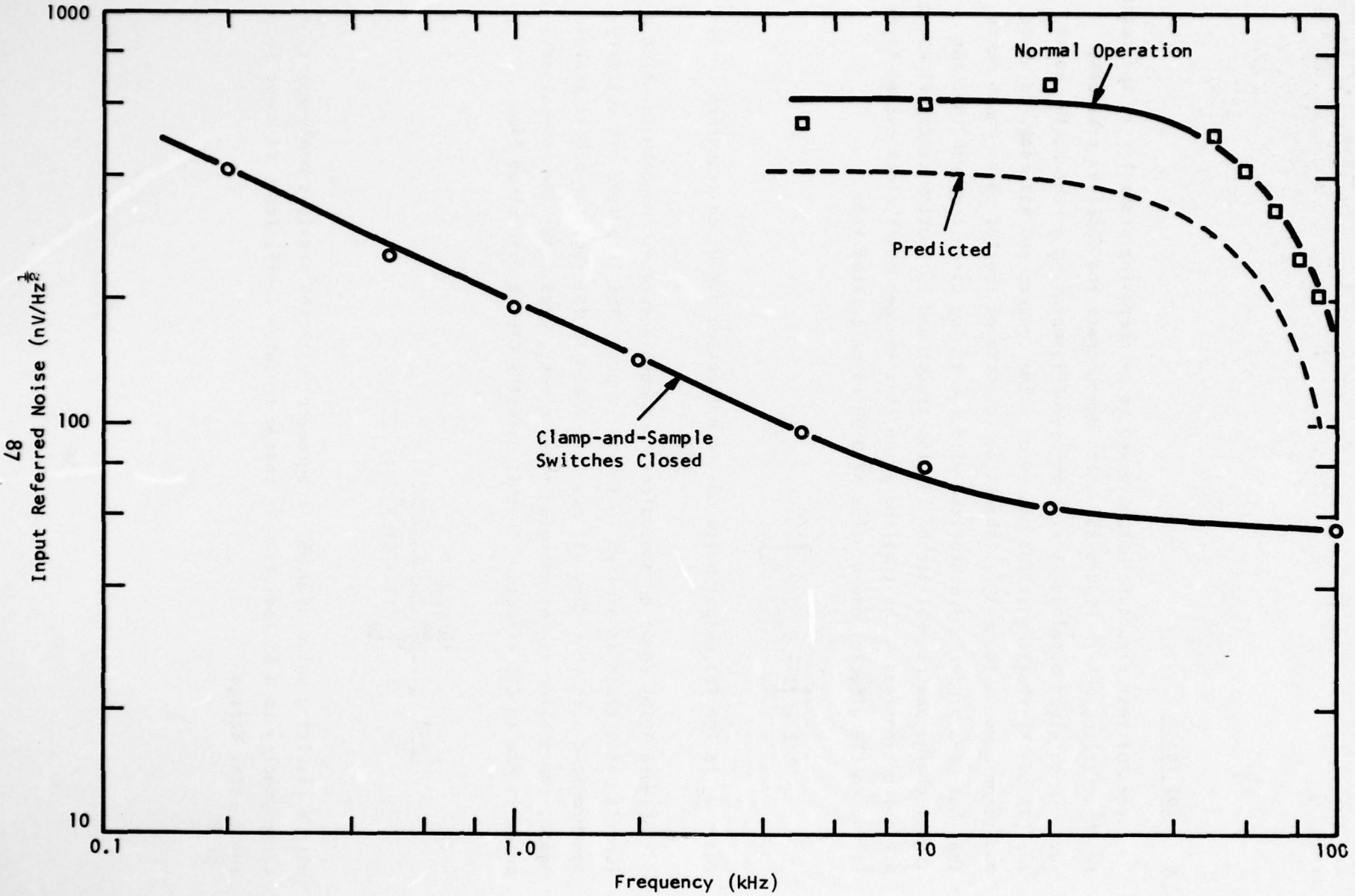


Figure 37 *Room Temperature Noise Performance of the CDS Test Circuit*

C. TDI Tests

The TDI test structure was observed to be operating properly, as indicated in the oscillograph in Figure 38, which demonstrate the familiar staircase waveform obtained obtained by time-delay-and-integrating a rectangular pulse. The CTE of the floating diffusions is of prime concern and was measured using two techniques. Figure 39(a) shows the response of the TDI to an input pulse that has been properly synchronized with the timing circuitry such that the signal charge packet experiences 10 (top trace) and 15 (bottom trace) floating diffusion transfers. The trailing pulse that emerges three clock cycles later is due to CTE effects, and a value of 0.99 is calculated from

$$CTE = \left[1 - V_{m+3}/V_m\right]^{1/n} \quad ,$$

where V_m is the TDI output pulse due to n floating diffusion transfers.

Figure 39(b) shows an equivalent, but more accurate, approach in which a 16-unit pulse train is applied to the TDI input. The 16 pulses are suitably synchronized such that they all sum into a single TDI register signal packet. Again, the smaller signal emerging three clock cycles after the main signal pulse is due to CTE effects. In this case the CTE is determined from

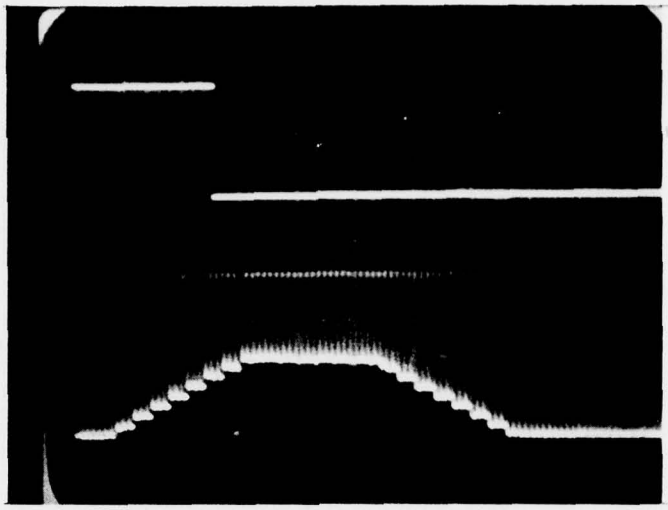
$$\frac{V_{m+3}}{V_m} = \frac{\sum_{n=1}^{16} (CTE)^n}{\sum_{n=1}^{16} (1 - CTE)^n} \quad ,$$

with a resulting value of 0.99, in agreement with the previous measurement, and corresponding to a 6X reduction in charge transfer inefficiency as compared to the initial design.

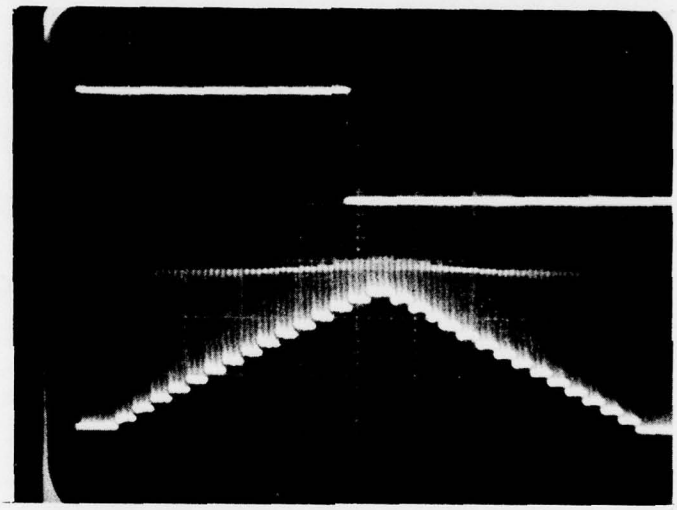
AD-A068 910 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 9/5
CCD PROCESSOR FOR INSB ARRAY.(U)
DEC 78 R J KANSY N00173-76-C-0237
UNCLASSIFIED TI-08-78-50 NL

2 OF 2
AD
A068910

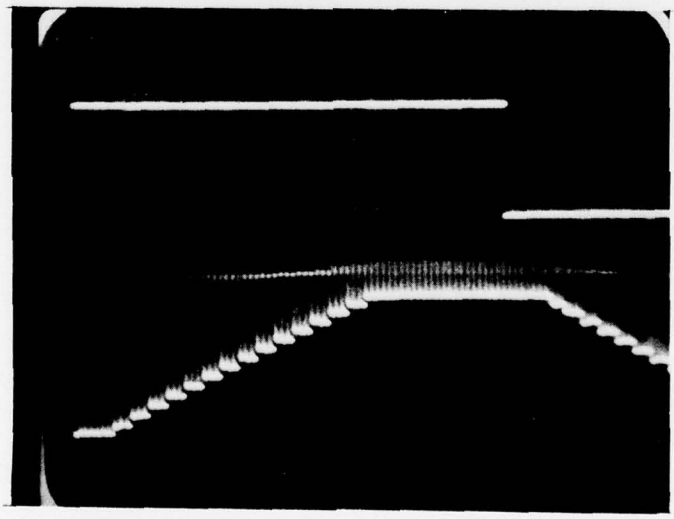
END
DATE
FILMED
6-79
DDC



< 48 cycles



48 cycles



> 48 cycles

Figure 38 Time Delay and Integration of a Rectangular Pulse
(Vert: 0.5 V/div; Horiz: 0.1 ms/div)

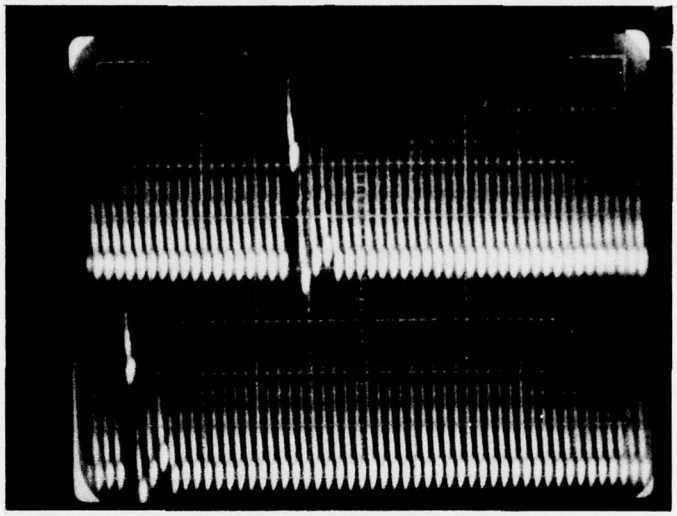


Figure 39(a) TDI Response Due to a Single Charge Packet
(Vert: 20 mV/div; Horiz 50 μs/div)

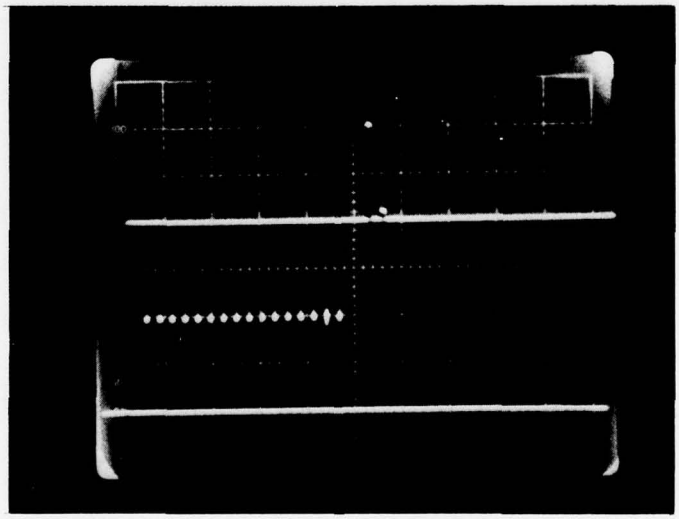


Figure 39(b) TDI Response Due to a 16-Unit Pulse Train
(Horiz 0.1 ms/div)

Operation of the new output diode in the demultiplexer was checked by inhibiting the clock pulse applied to the parallel transfer gate. In the previous design this resulted in "flooding" the demultiplexer channel and eventual spilling of charge over the parallel transfer gate and into the summing register. No charge spilling is observed in the present structure, indicating proper draining of the charge in the demultiplexer channel by the output diode.

Noise measurements at the TDI output indicate considerably higher noise levels than predicted. Previous calculation of the noise performance of the TDI indicated that it should be dominated by kTC noise, resulting in a wideband output noise level of less than 100 μV rms. However, these calculations neglected the floating diffusion "bucket-brigade" type transfer as a potential noise source. An analysis of the bucket brigade transfer mechanism shows that the variance in the number of charges transferred at each transfer is[24]

$$\langle \xi^2 \rangle = kTC_{FD}/q^2 \quad ,$$

where C_{FD} is the capacitance of the floating diffusion. The value of C_{FD} is calculated to be 0.069 pF from geometrical considerations, resulting in 106 noise electrons per transfer at room temperature. Since each consecutive charge packet contributing to a single TDI output charge packet experiences an additional transfer through a floating diffusion, the resulting variance on the output charge packet is

$$\langle \xi^2_{out} \rangle = \langle \xi^2 \rangle [1+2+3+...16] = 136 \langle \xi^2 \rangle \quad .$$

Since adjacent charge packets in the shift register are separated by two interleaved packets in the TDI register, a strong correlation will exist between charge packets

Q_n and Q_{n+3}, resulting in peaks in the noise spectral density at odd multiples of $f_{clock}/6$.

The expression for the single-sided noise spectral density as measured at the TDI output is

$$S(f) = \frac{2}{f_c} \left(\frac{q}{C_{out}} \right)^2 \langle \xi^2_{out} \rangle \quad (1 - \cos 6\pi f/f_c) \quad ,$$

where f_c is the TDI register clock rate and C_{out} is the value of the output node capacitance. The sinx/x aperture function of the sample-and-hold output has been neglected. Inserting the appropriate numerical values (C_{out} = 0.7 pF, f_c = 92.5 kHz) yields

$$S(f) = 1.73 \times 10^{-12} \quad (1 - \cos 6\pi f/f_c) \quad .$$

Figure 40 compares the noise spectrum measured at the TDI output for normal operation at room temperature with the expression above, and also shows the output circuit kTC noise level which was measured by disabling the TDI input circuit. The correspondence between theory and experiment is very good, and the bucket brigade transfer noise is positively identified by its unique spectral density function.

D. Multiplexer Tests

Operation of the redesigned 24-channel multiplexer at room temperature is demonstrated in the oscillograph of Figure 41(a), where a triangular test signal is applied at ac-coupled input number 13. Dc restoration was performed every 200 input cycles. Voltage gain through the structure is 0.14, which is still four times smaller than expected. Figure 41(b) is an expanded view of the

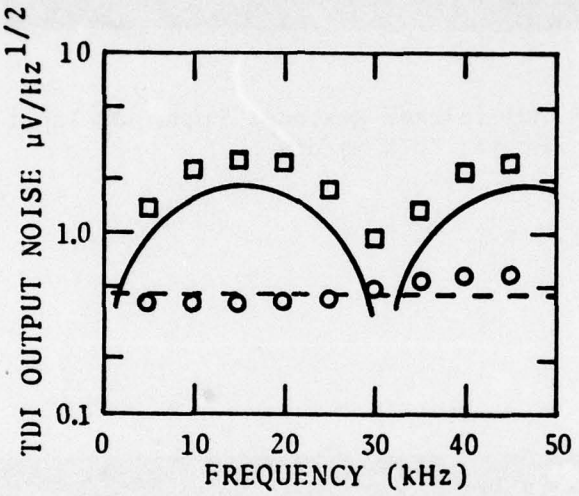


Figure 40 TDI Output Noise Spectrum. (Solid line: theoretical transfer noise. Dashed line: predicted kTC noise. Measured values are indicated by squares and circles, respectively).

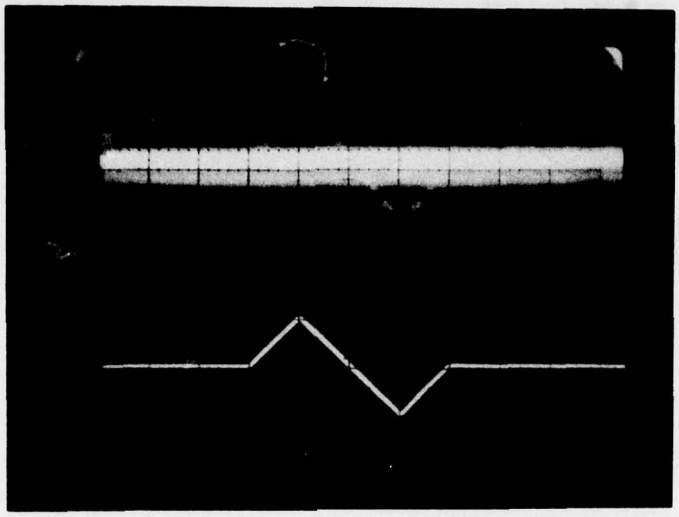


Figure 41(a) Multiplexer Response Signal at Input #13
Horiz: 0.2 ms/div

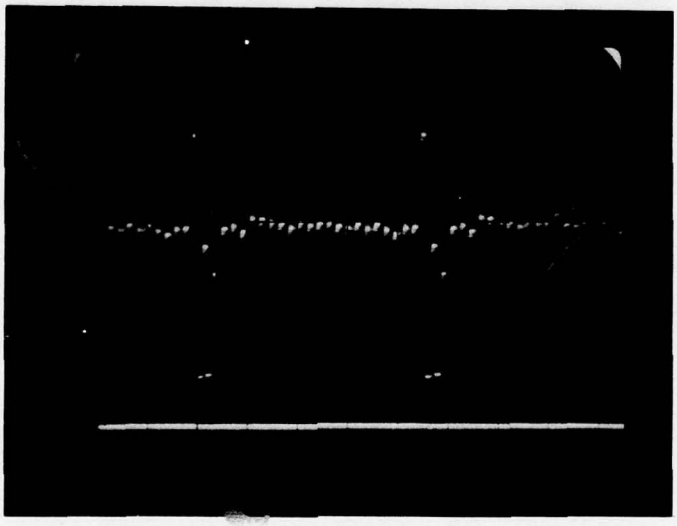


Figure 41(b) Multiplexer Response Detail
Horiz: 5 μs/div

output waveform illustrating the fixed pattern noise performance. Except for a large transient induced by the parallel transfer pulse (believed to be spurious coupling in the experimental set-up), the fixed pattern variations are within an input referred range of ± 100 mV. This is a dramatic improvement over the performance of the previous structure, but at least a factor of two larger than expected on the basis of worst-case threshold voltage variations. It appears that the potential barriers mentioned in the previous section have been reduced measurably, but not eliminated.

As in the TDI, the primary thermal noise source in the multiplexer is due to the bucket brigade transfers in the floating diffusion cells. CTE in the multiplexer has been improved substantially and is slightly better than observed in the TDI. The CTE was measured using the serial input circuit added in the redesign and was found to be approximately 0.994 at room temperature. This value is in good correspondence with previous calculations and should result in less than 1% crosstalk at 77 K.

The multiplexer structure has not been tested at low temperatures, although operation of the output buffer amplifier is expected to be degraded due to the use of fixed bias depletion mode load devices.

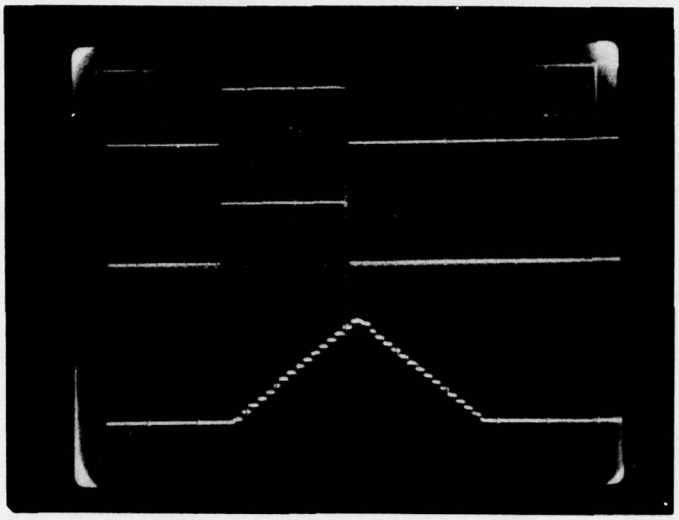
E. Processor Tests

Although evaluation of the processor chip has not been performed, preliminary evaluation of a single processor channel at 300 K has been accomplished by interconnecting the individual preamplifier, CDS, and TDI test structures on a test chip. These tests were performed to establish a baseline level of performance from which processor capabilities can be assessed.

The input waveform for these tests was generated with an external clamp/sample circuit to provide a reference level for the CDS clamp operation. This circuit utilized the reset and injection pulse waveforms generated in the processor timing circuit described in Appendix A. Although the test structures utilized were on the same chip, they were externally interconnected using coaxial cables, and the input sample rate was reduced to 148 kHz to accommodate the large parasitic load capacitances.

Figure 42(a) shows the input signal and CDS and TDI output waveforms corresponding to the maximum signal amplitude for linear operation of the TDI. The voltage gain through the preamplifier and CDS circuits is approximately 10 due to the extra source-follower in the preamplifier test structure and the high bias levels in the CDS source-followers required to obtain sufficient bandwidth. The dc reference level in the input waveform is coincident with the top horizontal line on the oscilloscope graticule.

Figure 42(b) shows the CDS and TDI output waveforms when the test signal is reduced in amplitude by 40 dB. The appearance of the TDI output waveform is due to droop in the sample-and-hold circuit connected to the TDI output in order to reduce clock feedthrough noise. This effect is shown in the expanded portion of the TDI output waveform. The wideband noise measured at the TDI output is approximately 520 μV rms and is generated within the TDI structure (confirmed by shorting the TDI input to ground). The primary noise component is due to the bucket brigade transfer mechanism discussed earlier, as was evidenced by observation of the characteristic noise spectral density function. The resulting dynamic range observed in the TDI is 65 dB (peak signal to rms noise). The wideband noise measured at the CDS output is 430 μV rms and is primarily due to aliasing of Johnson noise components in the preamplifier and CDS circuits.

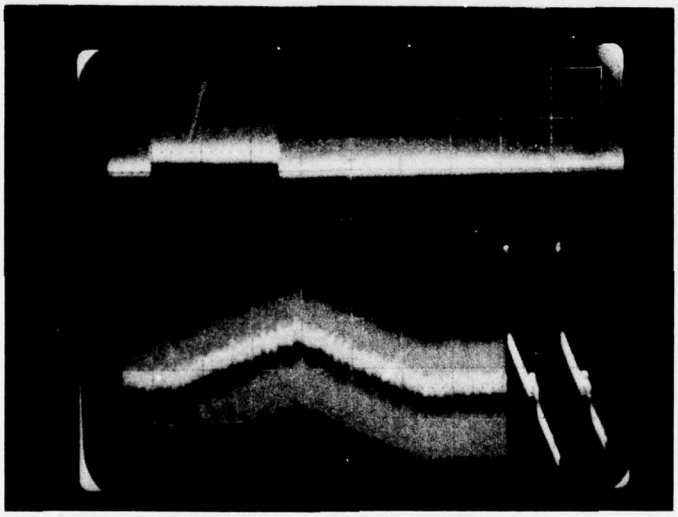


Input Signal
50 mV/div

CDS Output
500 mV/div

TDI Output
500 mV/div

Figure 42(a) Single Channel Test Circuit Response
f_s = 148 kHz, Horiz: 2 ms/div



CDS Output
20 mV/div

TDI Output
10 mV/div

Figure 42(b) Test Circuit Response -40 dB
Horiz: 2 ma/div, 100 µs/div

Although the noise performance of the processor channel test circuit is dominated by transfer noise generated in the TDI demultiplexer, the dominant noise sources in operation of the processor chip are in the output multiplexer. The capacitance of the floating diffusion cells in the multiplexer is calculated to be approximately 0.625 pF. The calculated transfer noise at the multiplexer output node is 450 μV rms at 77 K. Due to the extremely low voltage gain in the multiplexer, the transfer noise component dominates all other thermal noise sources in the processor by nearly two orders of magnitude.

The mechanism responsible for the low voltage gain in the multiplexer has not been isolated. Since the fixed pattern noise has been substantially reduced, it is believed that the remaining potential barriers are not of sufficient amplitude to cause the effect. Successful operation of previous CCD multiplexers suggests that the mechanism may be due to a peculiarity of the phase-multiplexed design that has not yet been comprehended.

SECTION VII
CONCLUSIONS

The approach taken to the design of the silicon processor chip involved the direct application of conventional analog MOS and CCD circuit techniques that had been previously applied in a number of successful programs executed at Texas Instruments. The success of the previous programs is primarily due to the establishment of an experimental data base relating processing and device parameters, which results in accurate risk assessment and a generally high level of confidence in new circuit designs. The disappointing results of this program are due, in part, to an inadequate understanding of this key concept. The program can be considered a success, however, in that it has resulted in the extension of the data base to include operation at 77 K. The risks associated with subsequent programs of a similar nature have been substantially reduced.

It is now apparent that low-risk MOS circuits for near-term cryogenic applications must incorporate enhancement mode, surface channel transistors exclusively. Further analysis of device behavior at low temperatures may result in the discovery of optimal implant profiles that are less sensitive to freeze-out effects, but this is quite beyond the scope of present efforts.

The neglect of the transfer noise component in the floating diffusion cells is potentially the easiest problem to correct. Full CCD implementation of the TDI demultiplexer will require higher clock rates and the potential for increased clock-to-signal crosstalk. The overall risk to processor performance is certainly lower than in the present configuration.

Implementation of the multiplexer with CCDs requires fanning the signal lines into the multiple input circuits. The concerns here include capacitive

balancing of the signal lines and clock crosstalk. Risk assessment in this case is not so straightforward, but better thermal noise performance is virtually guaranteed. Fixed pattern noise components in CCD multiplexers have been problematic to designers for years. The realities of tactical FLIR applications dictate an eventual analog-to-digital interface and raise the possibility of removing fixed pattern variations in the digital processor. The main requirement is that the fixed pattern offsets be sufficiently small--say, a few percent of the peak signal--so that the fixed word-length processor accuracy will not be degraded when the scene contrast is low.

In summary, although unexpected problem areas have been encountered, it is believed that low-risk alternatives can be developed. The results of this program indicate that, although further work is unquestionably required, analog NMOS/CCD circuits are the best candidates for on-focal plane signal processors with MIS detectors.

APPENDIX A

PROCESSOR TIMING CIRCUIT

APPENDIX A
PROCESSOR TIMING CIRCUIT

Schematic diagrams for the circuits designed to provide the necessary clock waveforms for the processor chip appear in Figures A-1 through A-3. The circuits were constructed using standard TTL components and utilized SN 75361 TTL/MOS converters to provide the high-level waveforms. The master clock waveforms (MC and $\overline{MC}$) were obtained from the Q and $\overline{Q}$ outputs of a J-K flip-flop, which is toggled at twice the desired clock rate with an external pulse generator.

The circuit in Figure A-1 generates the detector control, CDS, and high speed TDI clock pulses. Detector control and CDS clock pulses are derived combinatorily with a modulo 6 counter running at the master clock rate. The frequency of the MC waveform is 6X the desired operating rate, or about 9 MHz. The TDI demultiplexer input diode and two-phase clock waveforms are similarly generated. The TDI parallel transfer pulse, ϕ_{TS}^{TDI}, is enabled from the decoded output of a modulo 16 counter in Figure A-2. The resulting waveforms are sketched in Figure A-4. The ϕ_{TS}^{TDI} pulse occurs at a low duty cycle and is included in the figure to illustrate its relative timing.

The circuit shown in Figure A-2 generates the slower TDI clock and multiplexer input diode waveforms. A four-bit synchronous counter is clocked at MC/6 and is decoded by a 4-16 decoder to generate the desired sequence of pulses, which are then realigned with the MC waveform to eliminate differences in propagation delay.

The circuit in Figure A-3 generates the remaining multiplexer waveforms using a modulo 8 counter running at the master clock rate. The relative timing of the TDI and multiplexer clocks is illustrated in Figure A-5.

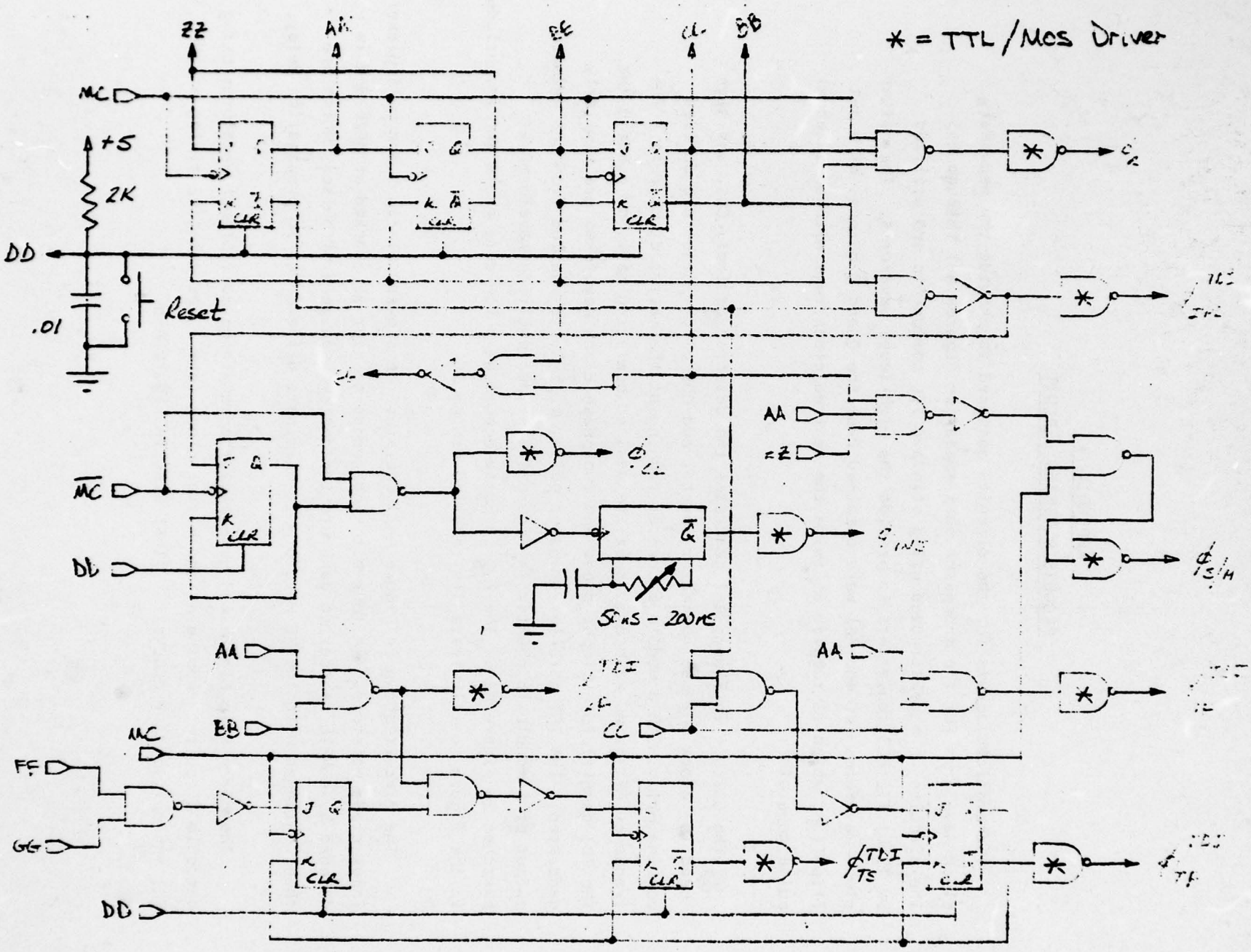

* = TTL / MOS Driver
ZZ
AA
EE
CC
BB
MC
+5
2K
DD
.01
Reset
AA
EB
CC
FF
GG
50nS - 200nS

Figure A-1

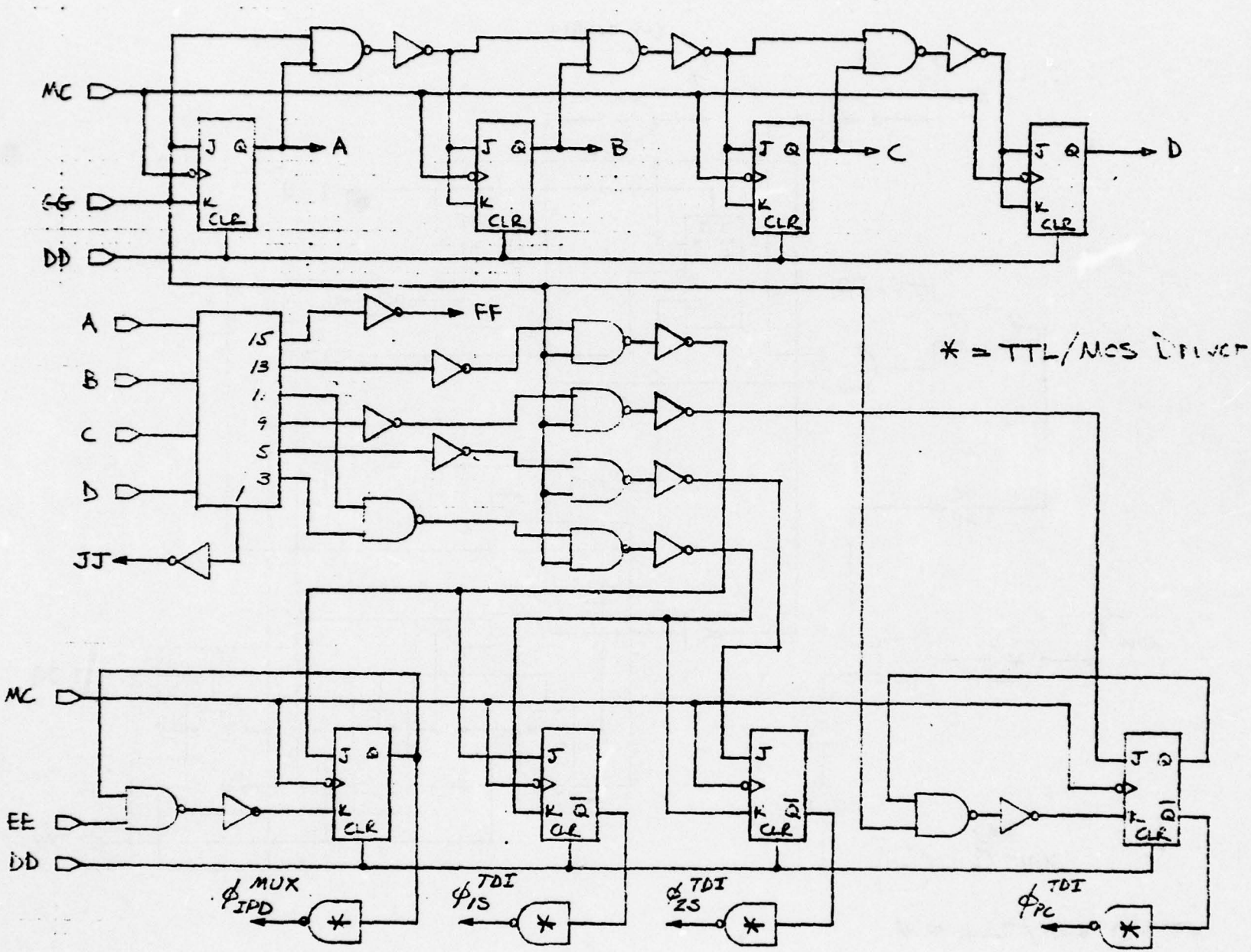

MC
GG
DD
J Q
K CLR
A
B
C
D
A
B
C
D
JJ
15
13
11
9
5
3
1
FF
* = TTL/MOS Driver
MC
EE
DD
J Q
K CLR
J
K Q̄ CLR
ϕ_{IPD}^{MUX}
ϕ_{IS}^{TDI}
ϕ_{ZS}^{TDI}
ϕ_{PC}^{TDI}

Figure A-2

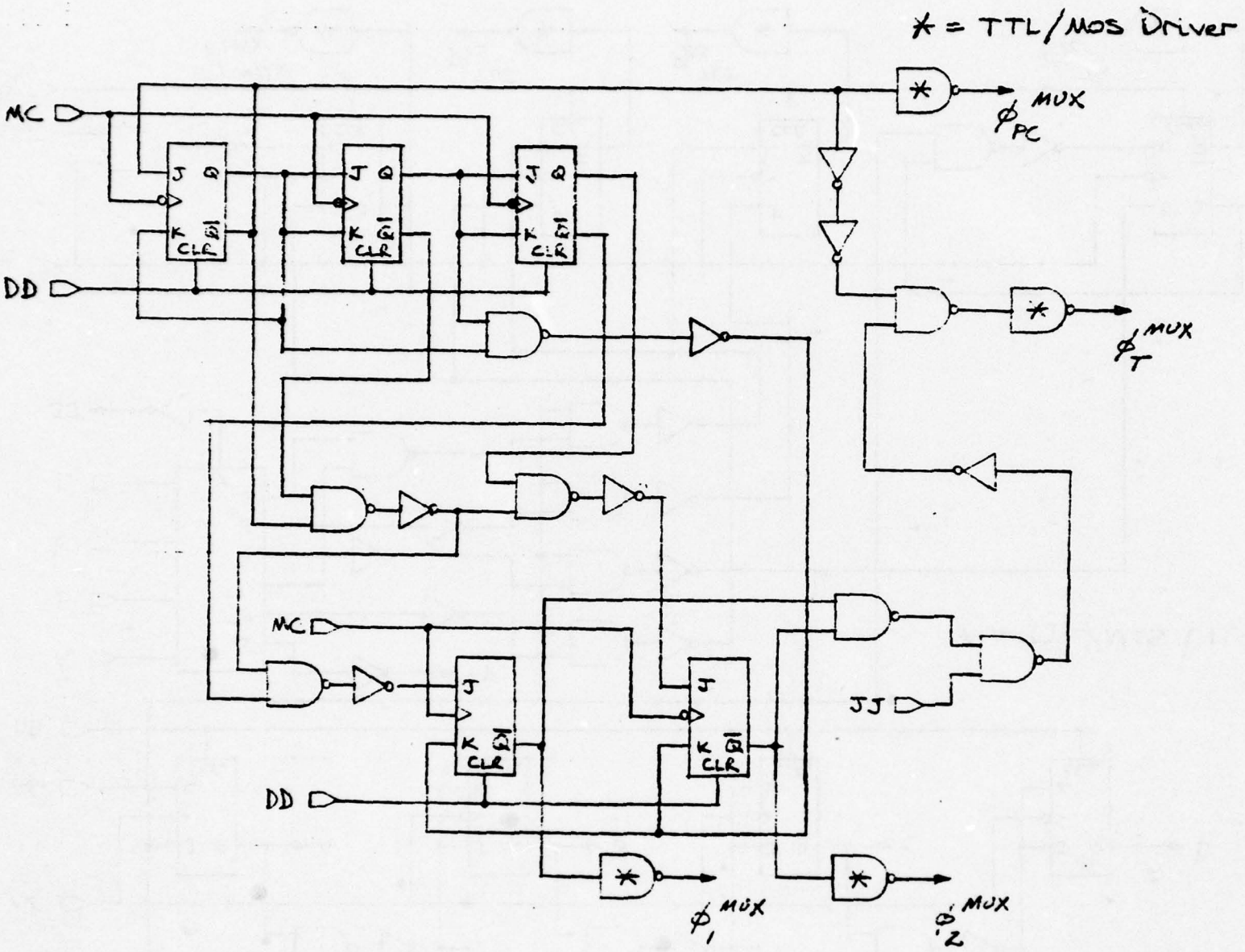


Figure A-3

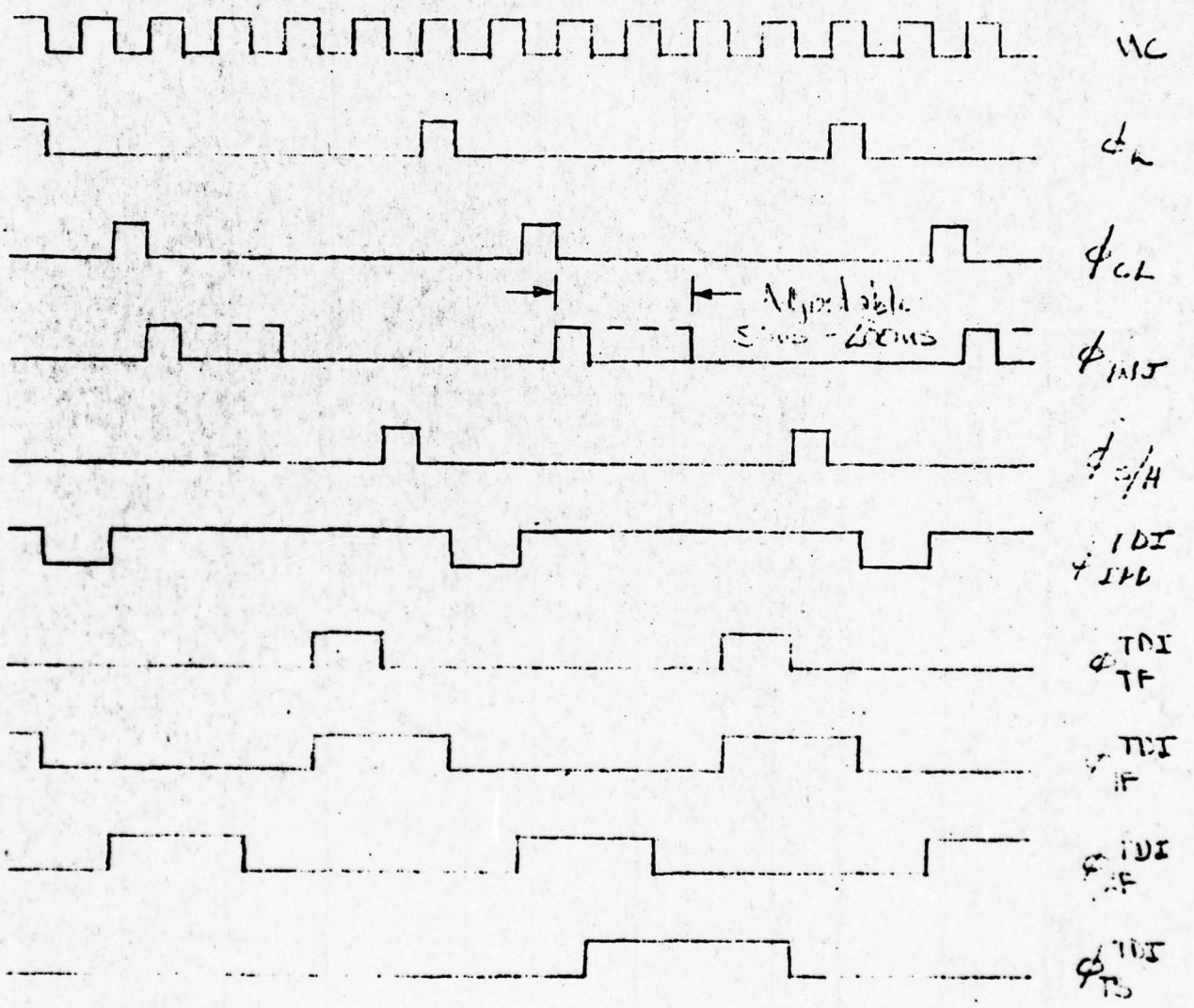


Figure A-4

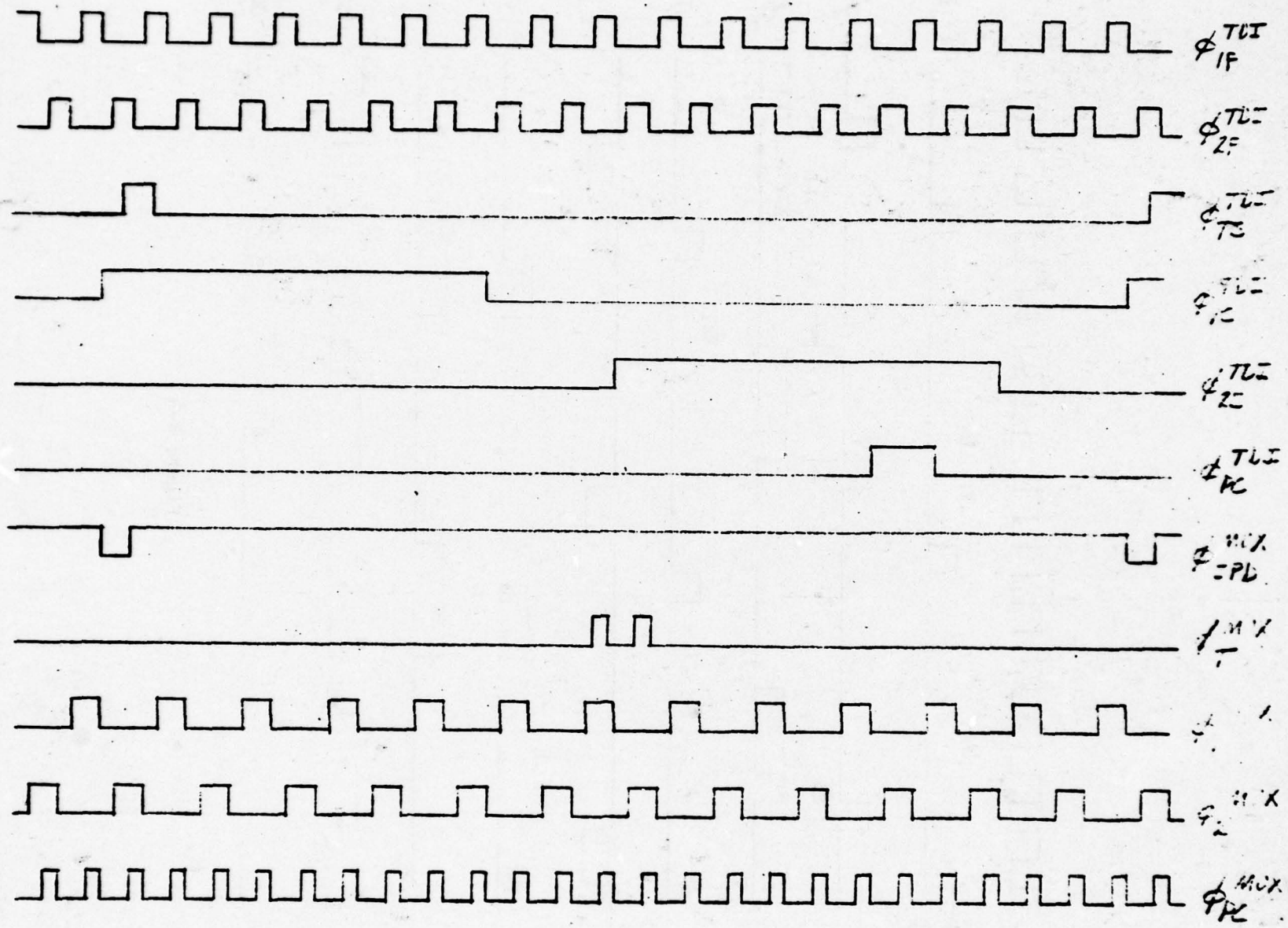


Figure A-5

APPENDIX B

LOW TEMPERATURE EFFECTS IN SURFACE CHANNEL DEPLETION MODE MOS TRANSISTOR

APPENDIX B

LOW TEMPERATURE EFFECTS IN SURFACE CHANNEL DEPLETION MODE MOS TRANSISTOR

The electric field in the surface depletion region of an enhancement mode MOS transistor maintains ionization of the substrate impurity atoms even when the bulk is frozen out. Thus, cryogenic application of enhancement mode MOS transistors is possible, and improved device performance is observed due to the temperature dependence of the mobility. Depletion mode MOS transistors can be fabricated by introducing a region of the opposite conductivity type near the semiconductor surface by ion implantation. The electric field in the surface depletion region confines the majority carriers in the implanted region near the surface, resulting in neutralization of the implanted impurities at low temperatures (freeze out). This causes a reduction in the fixed charge density in the channel and shifts the threshold voltage toward enhancement mode values, thereby reducing the drain current.

The MOS transistors fabricated in the silicon processor circuitry are n-channel units employing n^+ source and drain diffusions in a p-type substrate. Depletion mode devices are realized by introducing a thin n-type region in the channel by ion implantation. The ionized donor sites are positively charged and result in a negative threshold voltage of -3.5 to -4 volts at room temperature.

The extent to which the ionized donor density freezes out is determined by the proximity of the electron quasi-Fermi level, E_{fn}, to the donor level, E_D. The ionized donor density is given by

$$N_D^+(x, E_{fn}) = \frac{N_D(x)}{1 + 2\exp[-(E_D - E_{fn})]} \quad , \qquad (1)$$

where $N_D(x)$ describes the implant profile normal to the semiconductor surface (the x-direction).

The charge distribution in the semiconductor can be determined from Poisson's equation:

$$\frac{\partial^2 U}{\partial x^2} = \frac{q^2}{kT\epsilon_s}\left[n - p + N_A^- - N_D^+\right] \qquad (2)$$

$$= \frac{1}{2L_D^2}\left[\exp(U - \xi - U_F) - \exp(U_F - U) + N_A^-/n_i - N_D^+(x,U,\xi)/n_i\right],$$

where U is the electrostatic potential and U_F is the bulk Fermi level, both relative to the bulk intrinsic level and in units of kT/q. N_A^- and N_D^+ are the ionized acceptor and donor densities, respectively, and L_D is the intrinsic Debye length. Equation (1) can be written in terms of U, ξ, and U_F by observing that

$$E_D - E_{fn} = E_g/2 - E_d - (U - \xi - U_F) \quad , \qquad (3)$$

where E_g is the semiconductor energy gap and E_d is the donor level measured with respect to the conduction band edge. Thus,

$$N_D^+(x,U,\xi) = \frac{N_D(x)}{1 + 2\exp(U - \xi - U_F)\exp[(E_d - E_g/2)/kT]} \quad . \qquad (4)$$

Equation (4) is substituted into Equation (2), which can be solved numerically. The boundary conditions are

$$U = U_S \text{ at } x = 0,\ U = \frac{\partial U}{\partial x} = 0 \text{ at } x = \infty \quad , \qquad (5)$$

where U_S is the surface potential that is related to the gate voltage, V_G, by

$$V_G = \frac{kT}{q}U_S - \frac{Q_S(U_S,\xi)}{C_{ox}} \quad , \qquad (6)$$

and Q_S is the total charge in the semiconductor given by

$$Q_S = 2qn_i L_D (dU/dx)_{x=o} \quad . \tag{7}$$

$N_D(x)$ was obtained by fitting a curve to the experimentally measured "as-processed" implant profile. The electrostatic potential, $U(x)$, the electron density, $n(x,\xi)$, and the ionized donor density $N_D^+(x)$ resulting from solution of Equation (2) with $\xi = 0$ are plotted in Figures B-1, B-2, and B-3 with surface potential $U_S = U(0)$ as parameter. The metallurgical junction ($N_D(x) = N_A$) is located at $x = 0.27$ μm. For $U_S < 160$ kT/q the peak in the electron density is located in the semiconductor corresponding with the minimum in the potential, $U(x)$, due to the implant. The reduction in $N_D^+(x)$ also corresponds with the minima of $U(x)$, since these are regions of closest proximity of the donor level and the quasi-Fermi level.

Although a "flat-band" condition never strictly exists, a pseudo flat-band condition occurs for $U_S \sim 159$ kT for which $[\partial U/\partial x]_{x=o} = 0$. For values os $U_S > 160$ kT, the maxima of $U(x,\xi)$ occur at the oxide-semiconductor interface. Further increase in U_S results in formation of a surface charge sheet and little additional change in $N_D^+(x)$. This point is illustrated in Figure B-4, which shows the integrated implant and electron densities (Q_I and Q_n, respectively) as functions of the surface potential. These data were obtained by numerical integration of the data in the previous figures. It can be seen that for $U_S > 160$ kT/q, Q_I is approximately constant and equal to about 22% of the implanted charge.

As applied to the operation of a depletion mode transistor, the data in Figure B-4 are strictly valid only at the source, where $\xi = 0$. The overall impact on device performance can, however, be deduced. We consider only operation in the saturation region, since this is the typical mode of operation of a depletion load device. The saturation condition occurs when sufficiently

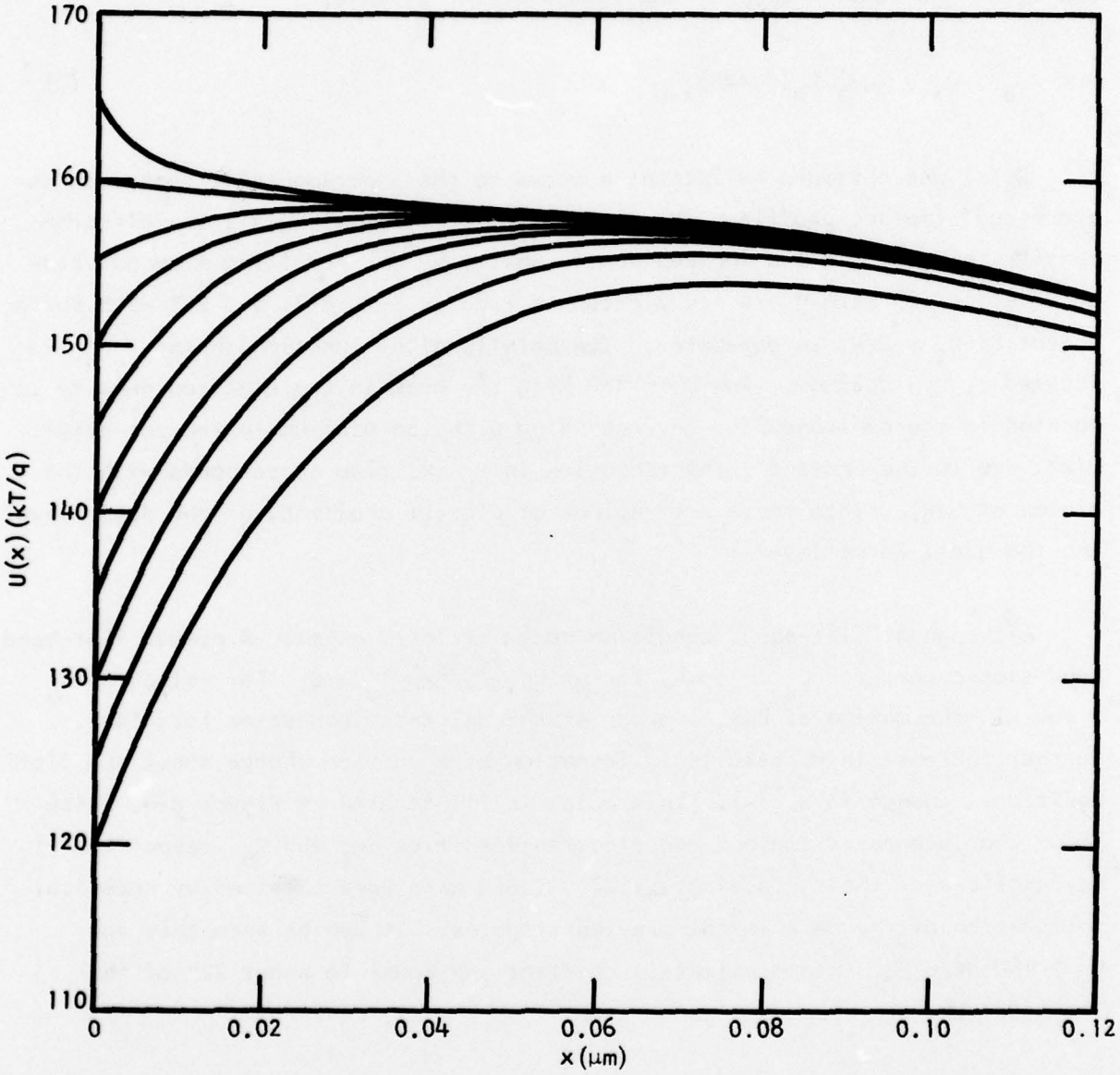


Figure B-1 Electrostatic Potential as a Function of x Near the Semiconductor Surface for $\xi = 0$

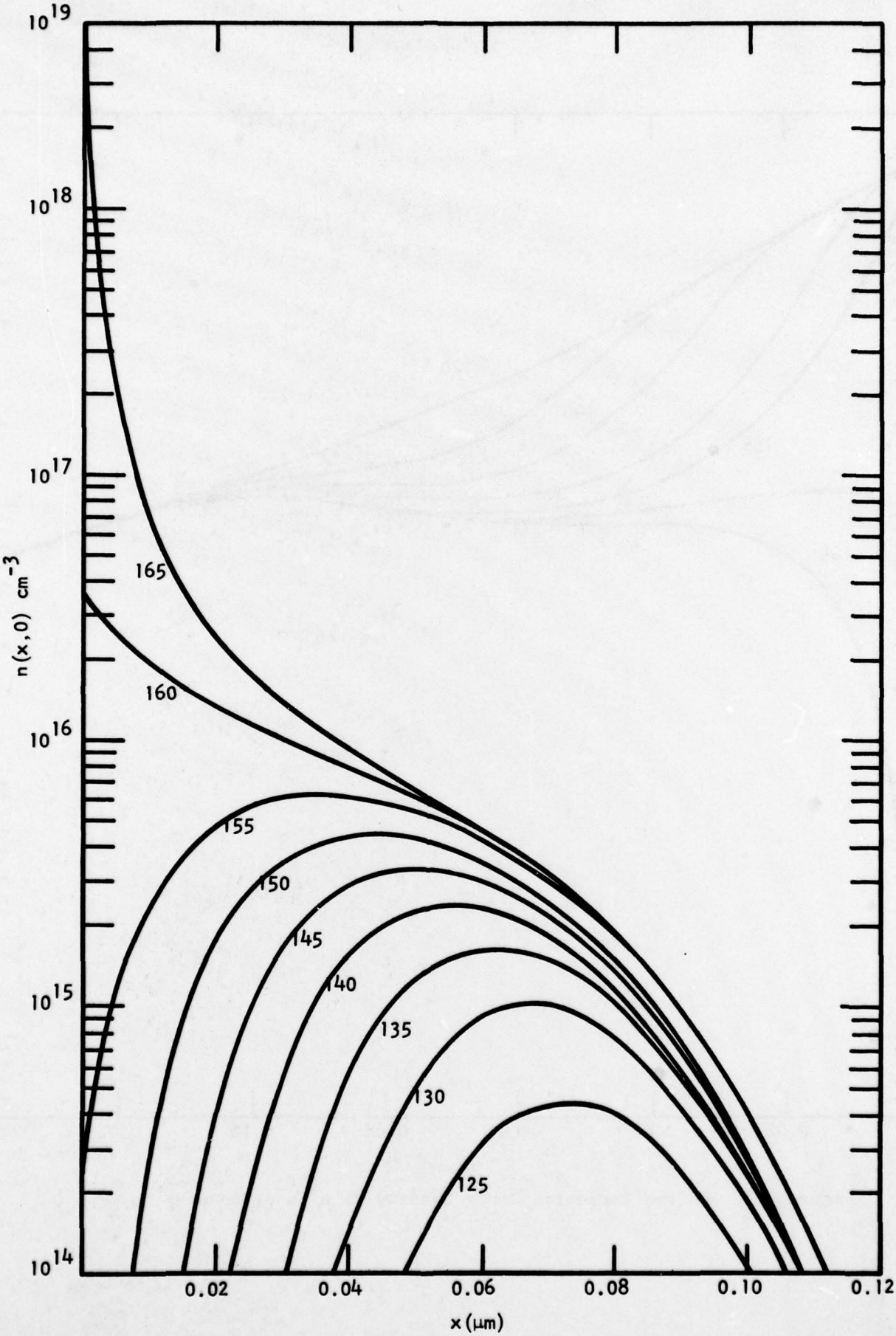


Figure B-2 Electron Density as a Function of x for $\xi = 0$

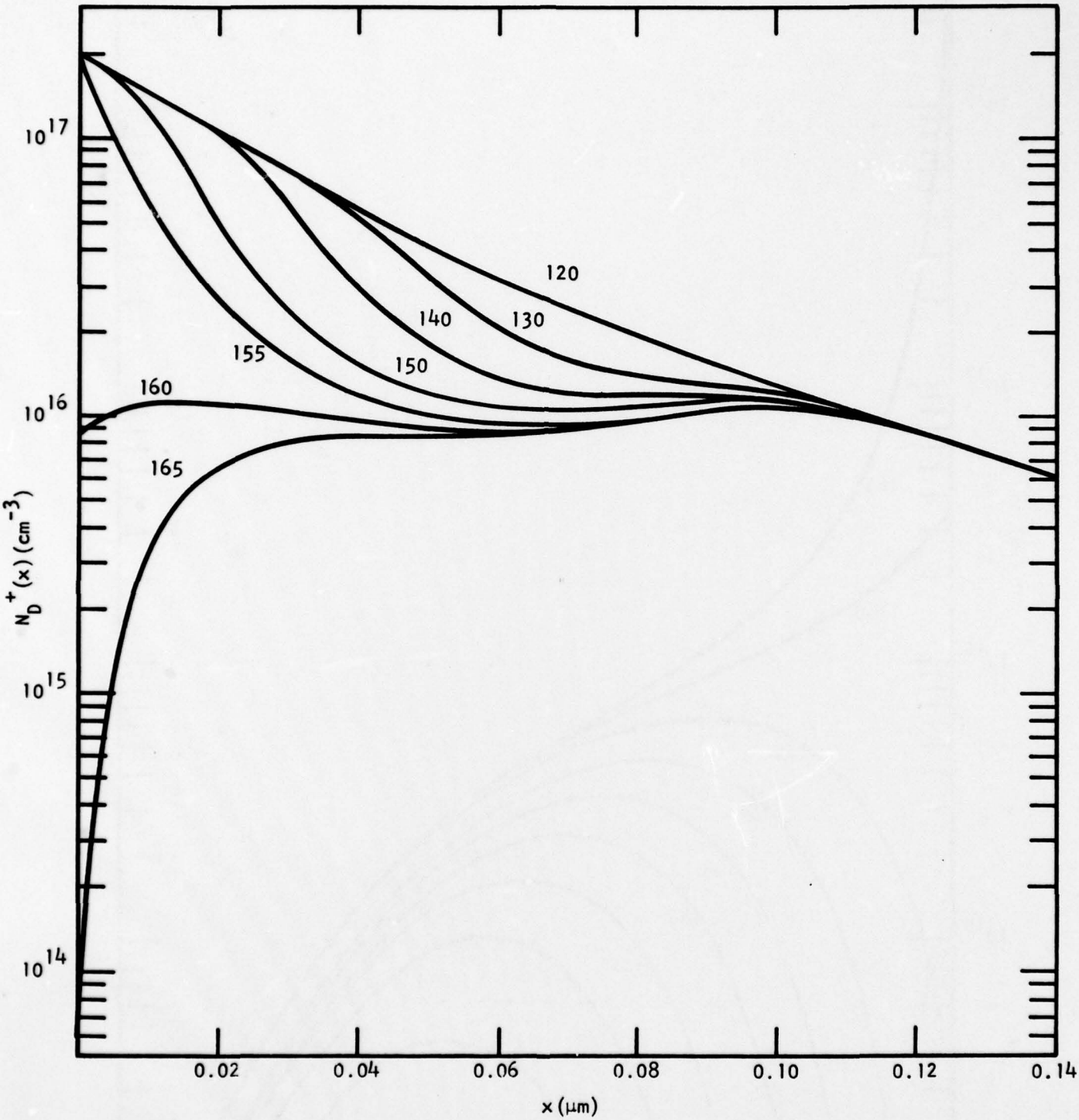


Figure 8-3 Ionized Implanted Donor Density as a Function of x for $\xi = 0$

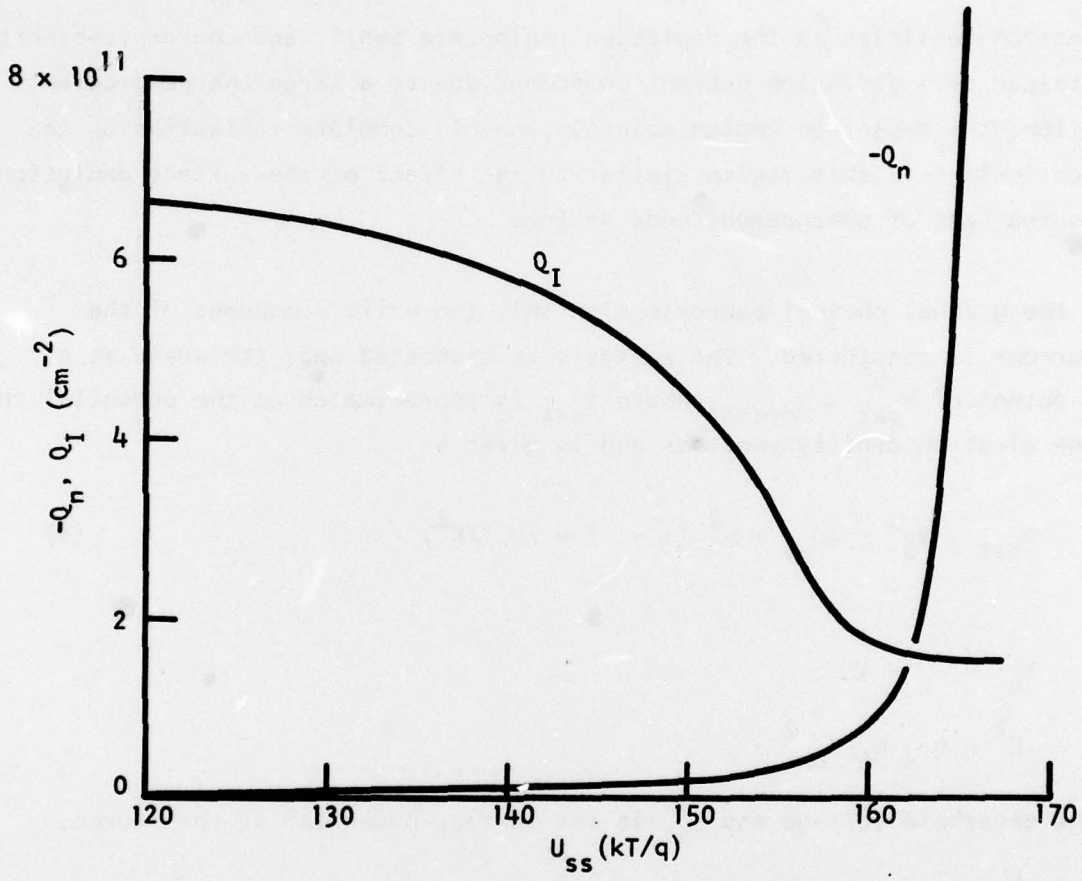


Figure B-4 Integrated Ionized Donor Density (Q_I) and Electron Density (Q_n) as a Function of the Surface Potential at the Source

large drain-source voltages are applied to cause extension of the drain depletion region into the conducting channel.

Electron densities in the depletion region are small, and charge transport is maintained by a diffusion current component due to a large charge gradient. In addition, the depletion region maintains nearly complete ionization of the depletion implant in this region similar to the effect of the surface depletion field in the case of enhancement mode devices.

In the gradual channel approximation only the drift component of the drain current is considered. The analysis is truncated near the drain at a channel potential $V_{sat} < V_{drain}$, where V_{sat} is approximated as the potential for which the electron density vanishes and is given by

$$V_{sat} = V_G' - 2\phi_{ss} + K^2 \left(1 - \sqrt{1 + 2V_G'/K^2}\right) \quad , \tag{8}$$

where

$$V_G' = V_G - V_T$$

$$K^2 = q\epsilon_s N_A / C_{ox}^2 \quad .$$

V_T is the threshold voltage and ϕ_{ss} is the surface potential at the source.

For small gate voltages (near V_T) Figure B-4 shows that the depletion implant is almost completely ionized at the source. Since V_{sat} is also small, similar conditions exist near the drain and the observed value of V_T should correspond closely with the fully ionized implant density.

Increasing the gate voltage results in a reduction of Q_I at the source. However, V_{sat} is still small and the donors in the drain region remain substantially ionized. Thus, Q_I is "averaged" over the channel resulting in a positive shift in V_T with gate voltage.

When large gate voltages are applied, formation of the charge sheet at the source results in a "screening" effect which inhibits further reduction in Q_I. However, the larger values of V_{sat} cause the electron distribution in the drain region to be shifted toward the oxide-semiconductor interface where the implant densities are largest. Thus, Q_I can be substantially reduced near the drain, although the drain depletion region is completely ionized. This mechanism involves the formation of a charge sheet, similar to that at the source, and V_T is expected to approach a constant value corresponding to the minimum value of Q_I in Figure B-4.

The threshold shift which should be observed at large gate voltages is calculated from Figure B-4 to be 2.4 V, in good agreement with Figure 36 of Section VI, which shows a 2.2 V shift between the theoretical value and that measured at 77 K.

REFERENCES

1. A. F. Milton and M. Hess, "Series-Parallel Scan IR CID Focal Plane Array Concept," Proceedings of 1975 International Conference on the Application of Charge Coupled Devices, San Diego, CA, October 1975, pp. 71-83.

2. F. H. Gaensslen, V. L. Rideout, E. J. Walker, and J. J. Walker, "Very Small MOSFET's for Low Temperature Operation," IEEE Trans. Electron Devices ED-24, 218 (1977).

3. B. Lengeler, "Semiconductor Devices Suitable for Use in Cryogenic Environments," Cryogenics 14, 439 (1974).

4. M. H. White, D. R. Lampe, F. C. Blaha, and J. A. Mack, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels," IEEE J. Solid-State Circuits SC-9, 1 (1974).

5. M. J. Chruchill and P. O. Lauritzen, "Carrier Density Fluctuation Noise in Silicon Junction FETs at Low Temperature," Solid State Electronics 14, 985 (1972).

6. A. F. Jordan and N. A. Jordan, "Theory of Noise in Metal Oxide Semiconductor Devices," IEEE Trans. Electron Devices ED-12, 833 (1967).

7. A. I. McWhorter, Semiconductor Surface Physics (Philadelphia, University of Pennsylvania Press, 1956), p. 207.

8. W. H. Fonger, "A Determination of 1/f Noise Source in Semiconductor Diodes and Transistors," Transistors I (RCA Laboratories, Princeton, N. J., 1956), p. 239.

9. S. Christenson, I. Lundstrom, and C. Svenson, "Low-Frequency Noise in MOS Transistors," Solid-State Electronics 11, 797 (1968).

10. R. W. Brodersen and S. P. Emmons, "Noise in Buried Channel Charge-Coupled Devices," IEEE J. Solid-State Circuits SC-11, 147 (1976).

11. This effect has been experimentally verified and is discussed in the final report on the buried channel MOSFET preamplifier development executed for the Air Force Avionics Laboratory under Contract F33615-76-C-1221.

12. W. Grant, R. Balcerak, P. VanAtta, and J. T. Hall, "Integrated CCD-Bipolar Structure for Focal Plane Processing of IR Signals," Proceedings of 1975 International Conference on the Application of Charge Coupled Devices, San Diego, CA, October 1975, pp. 53-58.

REFERENCES

(Continued)

13. D. M. Erb and K. Nummendahl, "Buried Channel Charge-Coupled Devices for Infrared Applications," Proceedings of the CCD Applications Conference, San Diego, CA, 1973, pp. 157-167.

14. D. D. Buss and W. M. Gosney, "The Effect of Sub-Threshold Leakage on Bucket Brigade Device Operation," presented at the 1972 Device Research Conference, Edmonton, Alberta, Canada, June 1972.

15. M. F. Tompsett, "Surface Potential Equilibration Method of Setting Charge in Charge-Coupled Devices," IEEE Trans. Electron Devices ED-22, 305 (1975).

16. T. F. Cheek, Jr., A. F. Tasch, Jr., J. B. Barton, S. P. Emmons, and J. E. Schroeder, "Design and Performance of Charge-Coupled Device Time-Division Analog Multiplexers," Proceedings of the CCD Applications Conference, San Diego, CA, 1973, pp. 127-139.

17. S. P. Emmons, A. F. Tasch, Jr., and J. M. Caywood, "A Low Noise CCD Input with Reduced Sensitivity to Threshold Voltage," IEEE International Electron Devices Meeting Technical Digest, Washington, December 1974, pp. 233-235.

18. R. L. Maddox, "p-MOSFET Parameters at Cryogenic Temperatures," IEEE Trans. Electron Devices ED-23, 16 (1976).

19. C. T. Sah, "Theory of Low Frequency Generation Noise in Junction-Gate Field-Effect Transistors," Proc. IEEE 52, 795 (1964).

20. L. D. Yau and C. T. Sah, "Theory and Experiments of Low-Frequency Generation-Recombination Noise in MOS Transistors," IEEE Trans. Electron Devices ED-16, 170 (1969).

21. J. W. Haslett and E. J. M. Kendall, "Temperature Dependence of Low-Frequency Excess Noise in Junction-Gate FET's," IEEE Trans. Electron Devices ED-19, 943 (1972).

22. T. I. Kamins, "Hall Mobility in Chemically Deposited Polycrystalline Silicon," J. Appl. Phys. 42, 4357 (1971).

23. S. M. Sze, Physics of Semiconductor Devices (Wiley-Interscience, New York, 1970).

24. D. D. Buss, W. H. Bailey, and W. L. Eversole, "Noise in MOS Bucket-Brigade Devices," IEEE Trans. Electron Devices ED-22, 977 (1975).

DISTRIBUTION LIST
CONTRACT N00173-76-C-0237

	Copies
W. D. Baker Code 5262 Naval Research Laboratory Washington, D.C. 20375	10
L. W. Sumney Code 3042 Naval Electronic Systems Command Washington, D.C. 20360	2
Jeffery Beck Honeywell Radiation Center 2 Forbes Road Lexington, Mass. 02173	1
Ronald A. Belt AFAL/DHE-1 Wright-Patterson AFB, Ohio 45433	1
Stephen B. Campana Code 20212 Naval Air Development Center Warminster, PA 18974	1
E. I. Gordon Bell Telephone Laboratories Murray Hill, N.J. 07974	1
Thomas Henion Advisory Group on Electron Devices 201 Varick St., 9th Floor New York, N.Y. 10014	4
Michael Hess Code 2022 Naval Air Development Center Warminster, PA 18974	1
Edward T. Hutcheson AMSEL-NV-FIR Night Vision Laboratory Ft. Belvoir, VA 22060	1

	Copies
J. C. Kim Bldg. 3, Room 201 General Electric Company Electronics Park Syracuse, N.Y. 13201	1
H. P. Leet Code 31505 Naval Weapons Center China Lake, CA 93555	1
A. Fenner Milton Code 5570 Naval Research Laboratory Washington, D.C. 20375	1
Milton Ritchie Code 3615 Naval Weapons Center China Lake, CA 93555	1
John Roschen Ford Aerospace and Communications Corp. Ford Road Newport Beach, CA 92663	1
Richard Thom Mail Stop 55 Santa Barbara Research Center 75 Coromar Drive Goleta, CA 93017	1
J. A. Tegnelia Tactical Technology Office Defense Advanced Research Projects Agency 1400 Wilson Blvd. Arlington, VA 22209	1
Ralph A. Rotolante Carson-Alexiou Minuteman Drive Sudbury, Mass. 01776	1
Commanding Officer Naval Research Laboratory Washington, D.C. 20375 Attn: Code 2627	6

	Copies
Defense Documentation Center Bldg. 5 - S 47031 Cameron Station Alexandria, VA 22314	12
Reliability Analysis Center RBRAC Griffiss AFB, New York 13441	1
James Merriam Code 2600 Naval Ocean Systems Center San Diego, CA 92152	1
Freeman Shepherd RADC/ESE Stop 30 Hanscom AFB, Mass. 01731	1